

OPERATING AND SERVICE MANUAL

**HP 59310B
BUS INPUT/OUTPUT
INTERFACE KIT**

Manual Part No. 59310-90068

Printed: APR 1978

HEWLETT  PACKARD

OPERATING AND SERVICE MANUAL

**HP 59310B
BUS INPUT/OUTPUT
INTERFACE KIT**

Manual Part No. 59310-90068

Printed: APR 1978

Card Assembly: 59310-60101
Date Code: 1812

LIST OF EFFECTIVE PAGES

Changed pages are identified by a change number adjacent to the page number. Changed information is indicated by a vertical line in the outer margin of the page. Original pages do not include a change number and are indicated as change number 0 on this page. Insert latest changed pages and destroy superseded pages.

Change 0 (Original) Apr 1978
All pages are original issue.

NOTICE

The information contained in this document is subject to change without notice.

HEWLETT-PACKARD MAKES NO WARRANTY OF ANY KIND WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Hewlett-Packard shall not be liable for errors contained herein or for incidental or consequential damages in connection with the furnishing, performance or use of this material.

This document contains proprietary information which is protected by copyright. All rights are reserved. No part of this document may be photocopied or reproduced without the prior written consent of Hewlett-Packard Company.

Copyright © 1978 by HEWLETT-PACKARD COMPANY

Library Index No.
59310-040-59310-90068

CONTENTS

Section I	Page	Status Word	3-6
GENERAL INFORMATION		Status Word Function	3-6
Introduction	1-1	Inputting the Status Word	3-6
Description	1-1	Status Word Coding	3-7
Identification	1-2	Data Output	3-9
Equipment Supplied	1-2	Data Transfer Capabilities	3-9
Specifications	1-2	Output Data Types	3-9
Software Available	1-2	Output Data Registers	3-9
Hewlett-Packard Interface Bus Capabilities	1-4	To Output Data	3-9
Program Code	1-4	Output Data Format	3-9
Addressing-Talking-Listening-Handshaking	1-4	Data Input	3-10
Functions of Instruments on the Bus	1-4	Data Transfer Capabilities	3-10
HP-IB Bus Lines	1-5	Input Data Type	3-10
Control Lines	1-5	Input Word Register	3-10
Data Lines (DIO1-8)	1-6	To Input Data	3-11
Transfer Lines	1-6	Input Data Format	3-11
Data Transfer	1-7	Flags	3-12
HP-IB Electrical Characteristics	1-9	Flag Organization	3-12
HP-IB Physical Characteristics	1-9	Main Flag	3-12
		End of Record Flag (EOR)	3-12
		Output Register Accepted Flag (ORA)	3-12
		Input Register Loaded Flag (IRL)	3-12
		Interface Clear Flag (IFC)	3-12
		Service Request Flag (SRQ)	3-12
		Serial Poll Mode Flag (SPM)	3-12
		DCPC Output Request Flag	3-13
		Machine I/O Instructions Operation	3-13
		Difference in Use of I/O Instructions	3-13
		STF Instruction	3-13
		OTA and OTB Instructions	3-13
		LIA, LIB, MIA and MIB Instructions	3-13
		SFS and SFC Instructions	3-13
		STC and CLC Instructions	3-13
		CLF Instructions	3-13
		ASCII Mode	3-14
		Enabling the ASCII Mode	3-14
		Operation When Outputting	3-14
		Operation When Inputting	3-14
Section II	Page	Section IV	Page
INSTALLATION		THEORY OF OPERATION	
Introduction	2-1	Introduction	4-1
Unpacking and Inspection	2-1	General Theory	4-1
Storage and Shipment	2-1	Control Word Processing	4-1
Environment	2-1	Bus Data Output	4-1
Installation	2-1	Computer Data Input	4-2
Power Requirements	2-1	Status Information Input	4-2
Programming of Hardwired Options	2-1	Detailed Theory	4-2
DIP Switches	2-2	Data Input/Output Control	4-2
Standard Mode of Operation	2-3	Control Word Processing	4-2
Installing Printed Circuit Board		Computer Data Input	4-3
in Computer	2-3	Status Information Input	4-5
Performance Check	2-3		
Interconnecting Cables	2-3	Section V	Page
Cabling Length Restrictions	2-3	MAINTENANCE	
Cabling Configurations	2-3	Introduction	5-1
		Troubleshooting	5-1
Section III	Page		
OPERATION AND PROGRAMMING			
Introduction	3-1		
HP Interface (HP-IB) Bus Lines	3-1		
Bus Functions Available to Computer	3-1		
Listen Functions	3-1		
Talk Functions	3-1		
Controller Functions	3-1		
System Controller Functions	3-2		
Communication Forms Between I/O PCA and			
Computer	3-2		
Control Word	3-2		
Functions and Modes	3-2		
Outputting the Control Word	3-4		
Control Word Group 1 Coding	3-4		
Control Word Group 2 Coding	3-5		
Control Word Group 3 Coding	3-6		

CONTENTS (continued)

Section VI	Page	Section VII	Page
REPLACEABLE PARTS		SCHEMATIC DIAGRAMS	
Introduction	6-1	Introduction	7-1
Ordering Information	6-1	Schematic Diagram Notes	7-1
HP Part Number Organization	6-3	Identification Markings on PC Boards	7-1
Component Parts and Materials	6-3	Component Locators	7-1

ILLUSTRATIONS

Title	Page	Title	Page
59310B Bus Input/Output Kit	1-1	Output Data Formats	3-10
HP-IB Bus Structure	1-5	Input Data Formats	3-11
Transfer Timing	1-8	Simplified Block Diagram	4-1
Pin Connections of the HP-IB Cables	1-10	Schematic Diagram Notes	7-2
Installation Information	2-2	59310B Block Diagram	7-3
Control Word Format	3-3	59310D Simplified Logic Diagram	7-5
Status Word Format	3-7	59310B Component Locator	7-9
		59310B Schematic Diagram	7-9

TABLES

Title	Page	Title	Page
59310B Equipment Supplied	1-2	Bus Cables	2-3
Specifications	1-3	Bus Line Nomenclature	3-1
Available Software	1-4	ASCII Modes Codes	3-14
Relation of ATN and Transfer (Handshake) Lines (NRFD, NDAC and DAV)	1-6	Reference Designations and Abbreviations	6-1
Summary of Bus Timing	1-7	Replaceable Parts	6-4
Power Requirements	2-1	Manufacturer Code List	6-7

GENERAL INFORMATION

SECTION

I

1-1. INTRODUCTION

This section provides general information on the Hewlett-Packard Model 59310B Bus Input/Output Interface Kit shown in figure 1-1. Included in this section are a description of the computer interface, card identification, equipment supplied, specifications and a description of the Hewlett-Packard Interface Bus.

(HP-IB). The HP-IB provides a two-way digital communications structure for one or more instruments with ASCII-compatible interface. Hardware connection of compatible instruments is a matter of plugging them together with the bus cables. Writing software programs for input/output operations to/from the computer is made easier by hardware features on the interface such as packing. Driver and utility subroutines for BCS and RTE (Real-Time Executive) are furnished as options to the 59310B.

1-2. DESCRIPTION

The HP 59310B Bus Input/Output Interface Kit interfaces the HP 1000 family of computers to the HP Interface Bus

The interface Printed Circuit Assembly (PCA) makes bus functions available to the computer: listen and talk functions, serial poll identification, controller clearing and



7700-175

Figure 1-1. 59310B Bus Input/Output Kit

four types of interrupt flagging. The 59310B also has parallel poll identification. Data transfers are byte-serial and bit parallel (8-bit bytes) and packing is available. Dual Channel Port Controller (DCPC) can be used for data transfers.

1-3. IDENTIFICATION

Printed-circuit assembly revisions are identified by a letter and a series code marked beneath the part number on the PCA. The letter identifies the revision of the etched-trace pattern on the unloaded PCA. The four-digit series code pertains to the electrical characteristics of the loaded PCA and component positions. If the series number does not correspond exactly with the series number on the title page of this manual, the PCA differs from the one described in this manual. These differences are covered in manual supplements available at the nearest HP Sales and Service Office listed at the back of this manual. In addition, there may be a suffix letter, e.g., (a), to indicate a minor circuit change which enhances operation.

1-4. EQUIPMENT SUPPLIED

Table 1-1 lists the equipment supplied with the Model 59310B Bus Input/Output Kit. The kit is shown in figure 1-1.

1-5. SPECIFICATIONS

Specifications for the 59310B Bus Input/Output card are provided in table 1-2.

1-6. SOFTWARE AVAILABLE

Software available for use with the 59310B is listed in table 1-3.

Table 1-1. 59310B Equipment Supplied

DESCRIPTION	STANDARD	OPT. 422	OPT. 423
Bus I/O PCA (Printed Circuit Assembly)	59310-60101	—	—
Cable Assembly	59310-60002	—	—
Tape Diagnostic	59310-16001	—	—
Operating and Service Manual	59310-90068	—	—
Diagnostic Manual	59310-90061	—	—
User's Guide	59310-90064	—	—
Tape, BCS Driver-D.37A (non-DCPC)	—	—	59310-60020
Tape, BCS Driver-D.37B (DCPC)	—	—	59310-60021
Tape, Bus Library	—	—	59310-60050
BCS Driver Manual	—	—	59310-90022
BCS Utility Subroutines Manual	—	—	59310-90050
Tape, RTE Driver-DVR37 (non-SRQ)	—	59310-16002	—
Tape, RTE Driver-DVR37 (SRQ)	—	59310-16003	—
Tape, RTE Utility Subroutines	—	59310-16004	—
RTE Driver Manual	—	59310-90063	—

Table 1-2. Specifications

ELECTRICAL CHARACTERISTICS

Bus Signal Lines: The Bus consists of 16 signal lines as follows:

DIO1	Data Input/Output 1
.	.
DIO8	Data Input/Output 8
DAV	Data Valid
NRFD	Not Ready for Data
NDAC	Not Data Accepted
IFC	Interface Clear
ATN	Attention
SRQ	Service Request
REN	Remote Enable
EOI	End or Identify

Logic Levels: High $\geq 2.4V$
Low $\leq 0.4V$

All signals are Low = True except NRFD and NDAC.

Line Termination: Each of the 16 Bus signal lines is terminated with $3K\Omega$ to Vcc and $6.2K\Omega$ to logic common. The value of Vcc depends on the particular 2100 series model in which the card is installed. It varies between 4.5 to 5.0V.

Line Drivers: The signal lines DIO1 through DIO8, DAV, ATN and EOI are drivers with a circuit having the following characteristics:

Type: Tri-State
Output Voltage Low State: $\leq 0.4V @ 48 \text{ mA}$
Output Voltage High State: $\geq 2.4V @ -40 \text{ mA}$

The signal lines NRFD, NDAC, IFC, REN and SRQ are drivers having the following characteristics:

Type: Open Collector
Output Voltage Low State: $\leq 0.4V @ 48 \text{ mA}$
Output Voltage High State: Determined by resistor termination
Leakage Current High State: $\leq 0.250 \text{ mA @ } 5.5V$

Line Receivers: Each of the 16 Bus signal lines is received with a circuit having the following characteristics:

Type: Schmitt Trigger
Threshold Positive Transition: 1.5V
Threshold Negative Transition: 1.1V
Input Current Low State: $-1.6 \text{ mA @ } 0.4V$
Input Current High State: $0.04 \text{ mA @ } 2.4V$

Maximum Cable Length: 2 metres per device connected, 20 metres total.

Operating Temperature: 0–55° Celsius

Power Requirements: The card requires the following amounts of power from the computer's power supply:

Supply	Maximum Current Acquired
+30	None
+12	None
+5*	3.0A
–2	100 mA
–12	None

*Value of supply varies from 4.5 to 5.0V depending on model of computer.

PHYSICAL CHARACTERISTICS

Card Dimensions:

Width: 7-3/4 in. (196,8 mm)
Height: 8-11/16 in. (220,7 mm)

Weight:

Net Weight, card and cable: 4 lb. (1,81 kg)
Shipping weight: 5 lb (1,94 kg)

Connector: 48-pin printed circuit board edge connector (cable supplied has standard bus connector on outboard end.)

Table 1-3. Available Software

MANUALS	
PART NO.	DESCRIPTION
59310-90022	Driver Program Procedure (BCS, D.37A/B)
59310-90050	BCS Bus Utility Subroutine
59310-90061	Diagnostic Program Procedure
59310-90063	Real-Time Executive System Driver (DVR37) Programming and Operating
59310-90064	User's Guide
59310-90068	Bus I/O Kit Operating and Service
SOFTWARE, BINARY PUNCHED PAPER TAPES	
59310-60020	BCS Bus I/O Card Driver, non DCPC (D.37A)
59310-60021	BCS Bus I/O Card Driver, DCPC (D.37B)
59310-60050	BCS Bus Utility Library (BLIB)
59310-16001	Bus I/O Card Diagnostic
59310-16002	RTE Bus I/O Card Driver, non-SRQ (DVR37)
59310-16003	RTE Bus I/O Card Driver, SRQ (DVR37)
59310-16004	RTE Bus Utility Library

1-7. HEWLETT-PACKARD INTERFACE BUS CAPABILITIES

HP-IB provides the capability of connecting from one to 14 compatible devices to the computer via one interface PCA. Data is transferred over the Bus bidirectionally in 8-bit bytes. Data can be transferred from a device to the computer or from the computer to one or more devices simultaneously or from one to other devices under the direction of the computer.

Some bus features must be used while others are optional. For example, all instruments must be capable of being addressed, but they may or may not be capable of being operated by remote control. A system may have some instruments operating under remote control while other instruments obey their front and rear panel controls (LOCAL). The same pins of all bus connectors of all instruments are connected in parallel making a parallel communication network. This permits information to flow in any direction on the bus and allows any instrument to talk directly with another without going through a central control unit.

1-8. PROGRAM CODE

Once a system has been assembled, programming is simplified since almost all HP instruments use the same code set. The seven-bit ASCII code set was selected because of its wide acceptance in the communications and data handling fields. The HP-IB itself can transmit full eight-bit binary data however. All of these features make the job of interconnecting instruments into a system simple. The job has been reduced primarily to programming.

1-9. ADDRESSING-TALKING-LISTENING-HANDSHAKING

A technique of addressing is used to determine which instrument is to "talk" and those instruments that are to "listen". Data is sent from one instrument to another one character (byte) at a time using an interlocked "Handshake" technique. This technique assures that the sender does not remove data before the receiver has finished using the data. It also insures that data is not lost when instruments having inherently different speeds communicate on the same bus.

1-10. FUNCTIONS OF INSTRUMENTS ON THE BUS

Instruments connected to the bus may function in one or more of the following ways: (They function only after being addressed.)

TALKER—Any instrument that is capable of sending or transmitting information on the bus. There can be *only one talker* at a time on the bus.

LISTENER—Any instrument that is capable of receiving or accepting information on the bus is a listener. There may be up to 14 listeners at the same time on the bus.

TALKER-LISTENER—An instrument has the capability of both sending and receiving information on the bus as defined above is both a talker and a listener. For example: a counter is a talker when sending data to a recorder and it is a listener when it is being programmed.

CONTROLLER—Any device that has been programmed to have the responsibility of managing the flow of information between instruments connected to the bus is a controller. It is capable of addressing one of the instruments as a *talker* and one or more as a *listener*. It is a *talker* and may be a *listener*. The HP interface bus permits a system to have more than one controller, but only *one* may be active at any time. (A controller can be contained within the System Controller.)

SYSTEM-CONTROLLER—The system designer must designate one instrument as the System Controller at the time the system is configured. This instrument performs

all the functions of a Controller plus it has the ability to gain absolute control of the Bus for programming instrument modes, collecting and processing data, etc.

1-11. HP-IB BUS LINES

The HP-IB Bus structure consisting of 16 signal lines is shown in figure 1-2. There are eight additional bus conductors: one ground, one cable shield and six twisted pair commons for six of the signal lines.

All sixteen signal bus lines have been given names and mnemonic acronyms that describe the message being carried on that line. There are three types of lines: Data (8), Transfer (handshake) (3), and Control (management) (5).

NOTE

All instruments connected to the bus, including the controller, must conform to these descriptions.

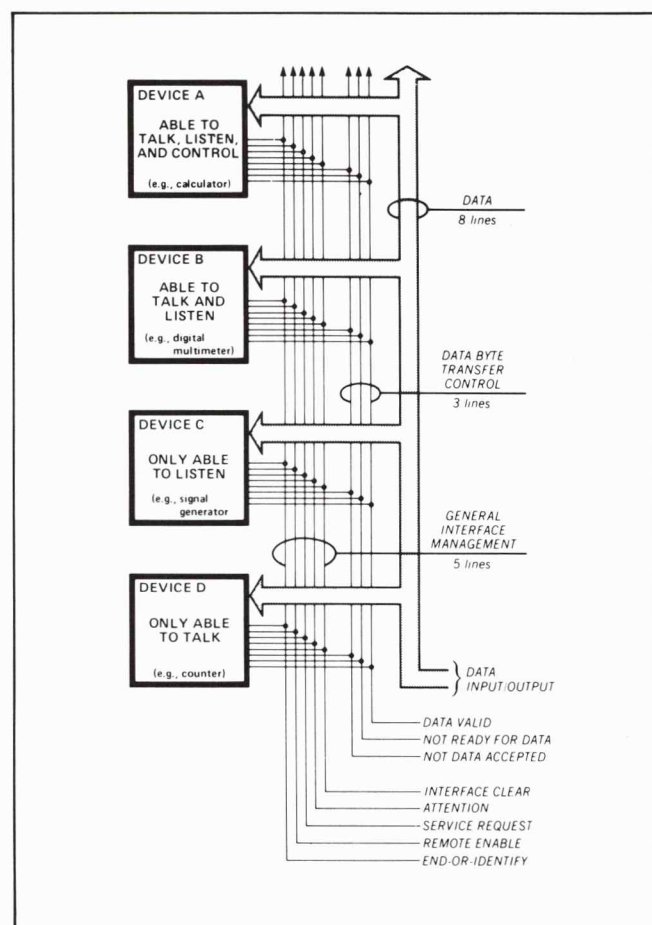


Figure 1-2. HP-IB Bus Structure

1-12. CONTROL LINES

The five control lines are used to manage the flow of information over the data and transfer lines. They communicate control and status information between the active controller and instruments connected to the bus. All instruments must use ATN and IFC. An instrument may or may not use REN, SRQ and EOI.

ATN (Attention) is driven by the active controller to place the bus in either the COMMAND (Low) or DATA (High) mode. All other instruments *must* monitor ATN at all times.

When the controller sets ATN to its low state, the bus is in the Command Mode. The primary purpose of the Command Mode is to permit the controller to send commands or address those instruments that are to communicate when the bus is placed in the Data Mode. Also, the controller may send "universal commands" while the bus is in the Command Mode.

When the controller puts ATN to its high state, the bus is in Data Mode. The instrument that was addressed to *talk* and those that were addressed to *listen* will now communicate on the Data Lines.

ATN may be set low or high at any time by a controller, however, it is usually changed at the end of a transfer (handshake) cycle so that data information is not lost. Timing of the transfer lines with respect to ATN is given below under Transfer Lines.

IFC (Interface Clear) is used by the system controller to initialize the bus. Only the system controller can drive IFC and it *must* be monitored by all other units on the bus. When the system controller sets IFC low for at least 100 μ sec the following takes place: all talkers and listeners are stopped, serial poll mode is disabled, and control is returned to the bus controller. When IFC is high it has no effect on the bus operation. The system controller may set IFC low at any time.

REN (Remote Enable) is one of the conditions for operating instruments under Remote Control. Only instruments capable of Remote operation use REN and they monitor it at all times. Instruments that do not use REN terminate the line in a resistor load. The system controller driver REN may change its state at any time.

SRQ (Service Request) is driven to its low state by an instrument to indicate that it wants the attention of the controller. SRQ may be set low by an instrument at any time except when IFC is in the low state. Only the controller senses SRQ. Some instruments do not use SRQ but terminate it in a resistor load.

EOI (End or Identify) may be used to indicate the end of an instruments character string. When the bus is in the Data Mode (ATN is high), the addressed *talker* may indicate the end of its data setting EOI low at the same time it places the last byte on the Data Lines.

1-13. DATA LINES (DIO1-8)

The data lines are used to communicate all data including input, output and program codes, addresses control and status information between instruments connected to the bus. These data are passed one character (byte) at a time (i.e., byte serial and bit parallel) under control of the Transfer Lines. In most instruments these data are based on the 7-bit ASCII code set. Unused data lines terminate in a resistor load.

1-14. TRANSFER LINES

The three transfer (handshake) lines are used to execute the transfer of each byte of information on the data lines. All instruments use these lines and employ an interlocked "handshake" technique to pass information. This allows asynchronous data transfer without timing restrictions being placed on any instrument connected to the bus. Transfer of each byte is accomplished at the speed of the slowest instrument. The three transfer lines are: NRFD, NDAC, and DAV.

NRFD (Not Ready for Data) is the transfer (handshake) line that indicates all *listeners* are ready to accept information on the data lines. NRFD is driven by all *listeners* (all instruments when ATN is low and only by those instruments addressed to listen when ATN is high). It is sensed by *talkers*: the controller when ATN is low, and the instrument addressed to talk when ATN is high.

When NRFD is high, all *listeners* are unconditionally ready for data. The *talker* may, at its own time, put a byte of information on the data lines and set DAV low. When NRFD is low, one or more *listeners* are not ready for data.

When the controller sets ATN low, all instruments must set NRFD to its high state within 200 nanoseconds, i.e., if an instrument is "Ready for Data" it places NRFD to its high state and if it is "Not Ready for Data" it sets NRFD to its low state. When the controller sets ATN high, all instruments that have not been addressed to listen will not drive NRFD, those addressed to Listen will set NRFD to its high state within 200 ns.

A listener must not set NRFD low until it senses DAV is low. It may do so before or at the same time that it sets

Table 1-4. Relation of ATN and Transfer (Handshake) Lines (NRFD, NDAC and DAV)

MODE	ATN	NRFD		NDAC		DAV	
		LOW	HIGH	LOW	HIGH	LOW	HIGH
ADDRESS	LOW	One or more units not ready for data	All units ready for data	One or more units have not accepted data	All units have accepted data	Controller has valid data on DIO lines	Controllers data is not valid
		1. Driven by all units except controller 2. Sensed by controller 3. All units set NRFD and NDAC to valid state within 200 nanoseconds after ATN goes LOW				1. Driven by controller 2. Sensed by listeners 3. See DAV above for timing	
DATA	HIGH	One or more listeners not ready for data	All addressed listeners ready for data	One or more listeners have not accepted data	All addressed listeners have accepted the data	The addressed talker has valid data on lines	The addressed talker data is not valid
		1. Driven by all units addressed to listen. 2. Sensed by the unit addressed to talk. 3. All units not addressed will not drive. 4. All addressed listeners set both NRFD and NDAC to valid within 200 nanoseconds after ATN goes HIGH.				1. Driven by the instruments addressed to TALK 2. Sensed by all instruments addressed to LISTEN 3. See DAV above for timing.	

NDAC high. It must not return NRFD high until it senses DAV is high and may do so after, or at the same time that it sets NDAC low.

NDAC (Not Data Accepted) is the transfer line that indicates the acceptance of information on the data lines.

NDAC is driven by all *listeners*. That is, all instruments when ATN is low and only those instruments addressed to listen when ATN is high. It is sensed by *talker* and the controller when ATN is low and by the instrument addressed to talk when ATN is high.

When NDAC is high, all *listeners* have unconditionally accepted the byte of information that is on the data lines and no longer need it. The *talker* may, at its own time set DAV high, remove that byte of information and continue. When NDAC is low, one or more *listeners* has not accepted the information on the data lines.

When the controller sets ATN low, each instrument must set NDAC to its high state within 200 nanoseconds. When the controller sets ATN high, the instruments that have not been addressed to listen will not drive NDAC, those addressed to listen will set NDAC to its true state within 200 nanoseconds.

A *listener* must not set NDAC low until it senses DAV is high. It may do so before or at the same time that it sets NRFD high. It must not return NDAC high until it senses DAV is low and it may do so after or at the same time that it sets NRFD low.

DAV (Data Valid) is the transfer line that indicates the validity of information on the data lines.

DAV is driven by *talkers*: the controller when ATN is low and by the instrument addressed to talk when ATN is high. It is sensed by *listeners* and by all instruments if ATN is low and by those instruments addressed to listen when ATN is high.

When DAV is low, the states of data lines DI01 through DI07 are unconditionally valid and may be accepted by all listeners at their own time. DAV can only be driven low if NRFD and IFC are high. When DAV is high, the information on the data lines is not valid. DAV cannot be set high unless NDAC is high and NRFD is low.

The *talker* has the responsibility of allowing enough time for cable rise time and ringing. It does this with DAV. The controller after placing the bus in the Address Mode (sets ATN low) must wait at least one microsecond before setting DAV low. Of course it must not do so unless NRFD is high. In either the Address or Data Mode, a *talker* designed with open-collector circuits must not set DAV low for at least two microseconds after placing valid data at its output connector. Those designed with tri-state integrated circuits must wait at least 500 nanoseconds.

Table 1-5. Summary of Bus Timing

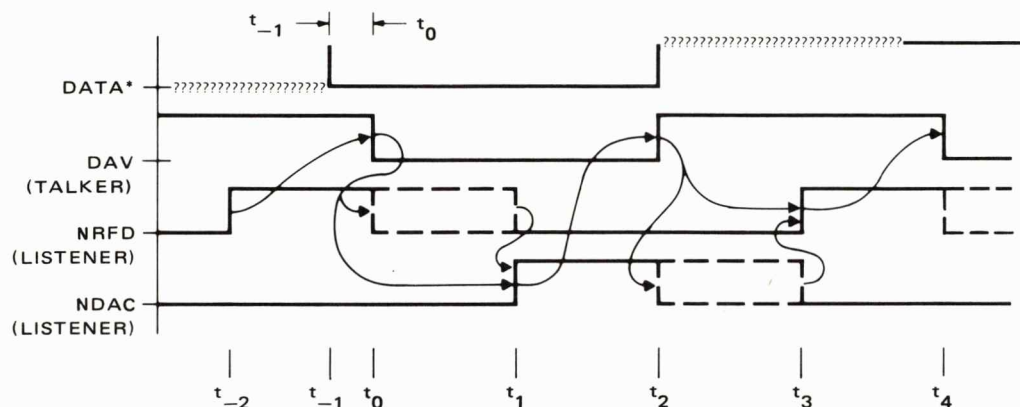
IFC INTERFACE CLEAR	The System Controller must set IFC low for at least 100 microseconds to clear the bus.
TRANSFER LINES WITH RESPECT TO ATN	<p>When sending an Address or a Universal Command the controller may set DAV low only after sensing that NRFD is high, and ATN has been low for at least one microsecond.</p> <p>When a controller changes ATN from its high to the low state or from low to high, all Listeners (all instruments when ATN is low and those addressed to Listen when ATN is high) put both NRFD and NDAC to their high state in less than 200 nanoseconds.</p>
TRANSFER LINES WITH RESPECT TO THE DATA	After changing the information on one or more Data Lines, the <i>talker</i> (the Controller when ATN is low or the instrument addressed to talk when ATN is high) must wait before setting DAV low. It waits $2 \pm \text{sec}$ if designed with open-collector circuits and 0.5 microsecond if designed with tri-state integrated circuits.

1-15. DATA TRANSFER

Transfer of data on the bus is asynchronous. It places no restrictions on the data rates of instruments connected to the bus. The timing and levels required to transfer a byte of information on the data lines are shown in figure 1-3. Transfer is under the control of three lines DAV, NRFD and NDAC. The *talker* (sender of data) drives the Data Lines and DAV (Data Valid) and the *listeners* (acceptors of data) drive both NRFD (Not Ready for Data) and NDAC (Not Data Accepted).

The transfer of a byte or data is initiated by all *listeners* signifying they are ready for data by setting NRFD high. When the *talker* recognizes NRFD is high and has placed valid data on the data lines it sets DAV low. When the *listener* senses that DAV is low and have finished using the data, they set NDAC high. Notice that the assertive or action state of both NRFD and NDAC is high. Since all

SEQUENTIAL REQUIREMENTS OF THE THREE WIRE TRANSFER



EVENTS

- t_{-2} : Listener becomes ready to accept data.
- t_{-1} : Talker has put data on the lines.
- t_0 : Indicates data is valid.
- t_1 : Listener has accepted the data and no longer requires it held valid.
- t_2 : Talker indicates the data is no longer valid and may change it.
- t_3 : Listener indicates it is ready for new data.
- t_4 : A new cycle begins (equivalent to t_0).
- t_{-1} to t_0 : Time that data is put on lines before DAV is set low.

*A composite of the DIO1 through DIO7 lines for illustrative purposes.
(The curved lines indicate interlocked signal sequence.)

Figure 1-3. Transfer Timing

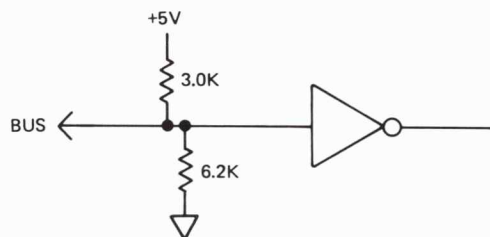
instruments on the bus have their corresponding lines connected together (e.g. NRFD), all *listeners* must be in a high state before that line goes high. This wire-AND situation allows a *talker* to recognize when the slowest listener has accepted a byte of data and is ready for the next byte.

Figure 1-3 also shows the timing of the transition to the non-assertive state of these lines. A *listener* may set NRFD low as soon as it recognizes that DAV has been set low and must do so before or at the same time it puts NDAC high. The *talker* may return DAV to its high state after it detects that NDAC is high. A *listener* may set NDAC low as soon as it recognizes that DAV is high and must do so before or at the same time it places NRFD in its high state.

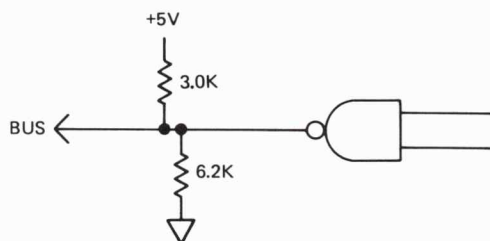
1-16. HP-IB ELECTRICAL CHARACTERISTICS

All 16 bus lines are designed to be compatible with TTL or DTL integrated circuits. Because wire-ANDING is used on some lines the line drivers must be either open collector or tri-state. Each line in every instrument is terminated in a resistor divider consisting of a $3\text{K}\Omega$ connected to 5V and a $6.2\text{K}\Omega$ connected to ground. Typically receivers are hex inverters and the drivers are open collector NAND gates. These may be put into four groups:

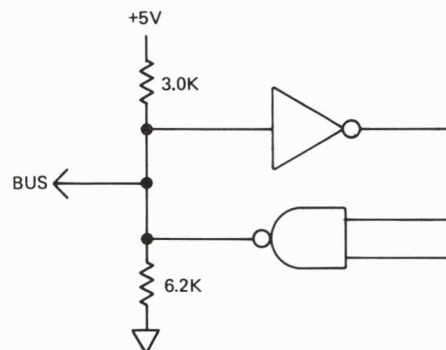
- Receivers only: They require -3.2 mA max. at 0.4V drive (A Standard Load).



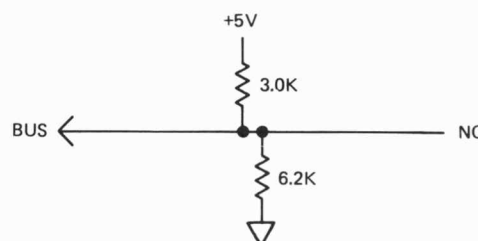
- Senders only: They are capable of sinking 45 mA at $+0.4\text{V}$ (A Standard Driver).



- Bi-directional Lines: They are a combination of the above, i.e., when a *talker*, capable of sinking 45 mA at 0.4V . When a *listener*, requires -3.2 mA at 0.4V to drive. Examples are the Data Lines (DIO1 through DIO7 for instruments using the ASCII code) and the handshake lines (NRFD, NDAC and DAV).



- Lines not used by an instrument are connected to a $3.0\text{K}\Omega$ resistor to $+5\text{V}$, and $6.2\text{K}\Omega$ resistor to signal ground (a Standard Termination). For example, DIO8 for instruments using the ASCII code or those not using REN, SRQ or EOI.



1-17. HP-IB PHYSICAL CHARACTERISTICS

Bus cables are available for connecting instruments into a system. These have one overall shield to reduce susceptibility to external noise. The cables use a mixture of individual wires and twisted pairs to reduce crosstalk. Both ends are identical. They are terminated in two 24-pin piggy back connectors; one male and one female. Pin connections of these connectors are shown in figure 1-4.

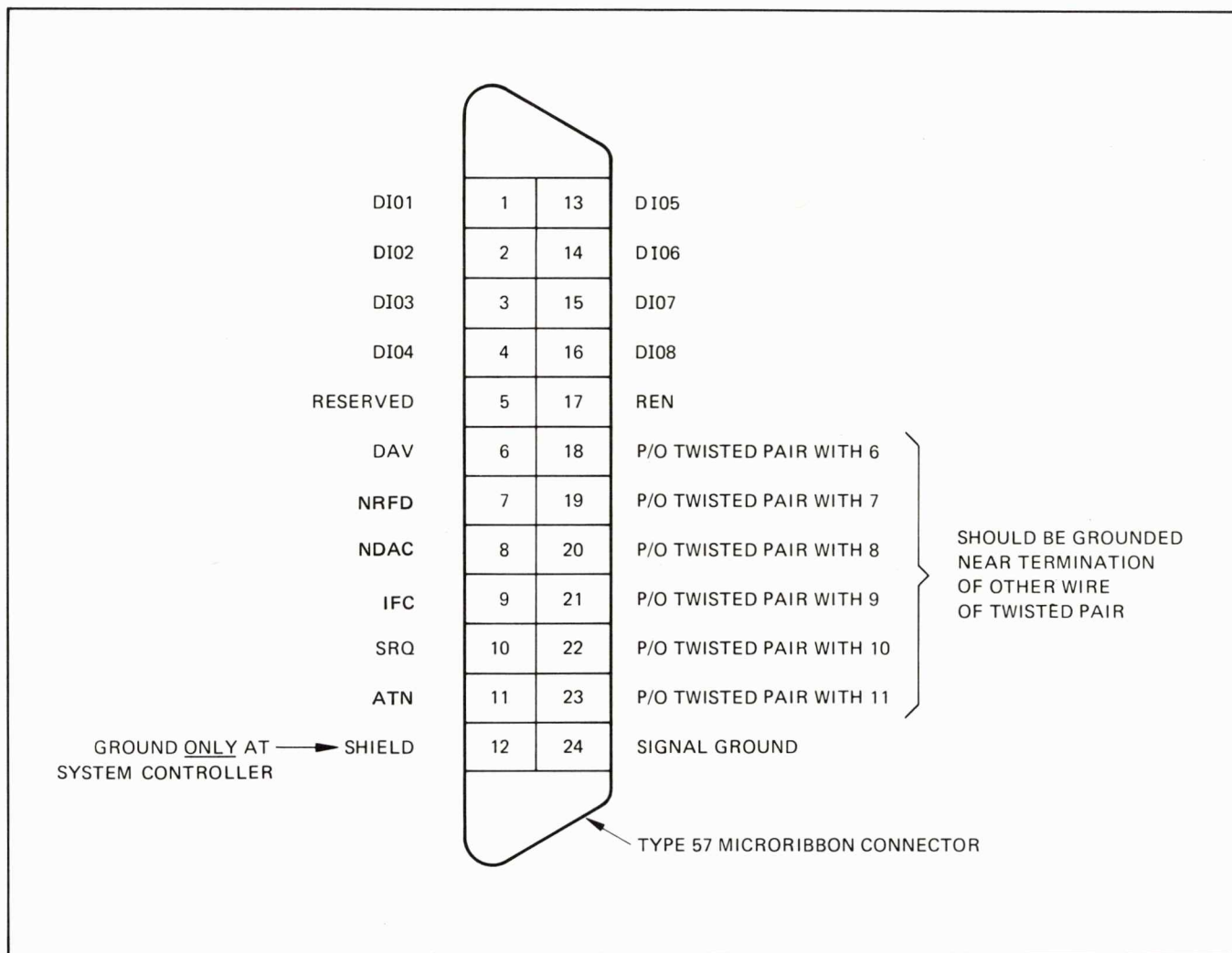


Figure 1-4. Pin Connections of the HP-IB Cables

2-1. INTRODUCTION

This section contains information for unpacking, inspection, repacking, storage, and installation. Information on the performance check and interconnecting cables is also included.

2-2. UNPACKING AND INSPECTION

If the shipping carton is damaged, ask that the carrier's agent be present when the carton is opened. Inspect the components for damage. If there is physical damage or the interface fails to meet electrical specifications, notify the carrier and the nearest Hewlett-Packard Sales and Service Office immediately (offices are listed at the back of this manual). Retain the shipping carton and padding material for the carrier's inspection. The sales and service office will arrange for the repair or replacement of your Bus I/O Interface Kit without waiting for the claim against the carrier to be settled.

2-3. STORAGE AND SHIPMENT

To protect the Bus Input/Output PCA (Printed Circuit Assembly) during storage or shipment, good commercial packing methods should be used. Reliable commercial packing and shipping companies have the facilities and materials to adequately repack an instrument.

NOTE

Before returning any product or component to Hewlett-Packard, contact the nearest Hewlett-Packard Sales and Service Office for instructions

2-4. ENVIRONMENT

Conditions during storage and shipment should normally be limited as follows:

- Maximum altitude: 25,000 feet.
- Minimum temperature: -40°F (-40°C).
- Maximum temperature: $+167^{\circ}\text{F}$ ($+75^{\circ}\text{C}$).

2-5. INSTALLATION

The following steps are suggested for preparing and installing the Bus Input/Output PCA into the computer:

- Determine that the computer has sufficient power to support the addition of the Bus Input/Output PCA. (Refer to paragraph 2-6.)
- Set up the hardwired options on the PCA using switches or jumpers for desired system functions. (Refer to paragraph 2-7.)
- Install printed circuit board assembly in computer. (Refer to paragraph 2-10.)
- Verify proper operation using the Diagnostic Program. (Refer to paragraph 2-11.)
- Interconnect system observing cabling restrictions. (Refer to paragraph 2-13.)

2-6. POWER REQUIREMENTS

Before installing the Bus Input/Output PCA in the computer, determine that the additional power consumed will not overload the computer power supply. The power required by the PCA is given in table 2-1.

Table 2-1. Power Requirements

SUPPLY VOLTAGE	MAX. CURRENT REQUIRED
+30	None
+12	None
+5*	3.0 A
-2	100 mA
-2	None
*Nominal value of voltage can vary between 4.5 to 5.0 volts depending on the computer model.	

2-7. PROGRAMMING OF HARDWIRED OPTIONS

Before installing the Bus I/O PCA in the computer, several "options" must be programmed for the desired user application and system function by use of DIP switches.

The DIP switches allow easy changing of the card's function to accommodate changing system requirements.

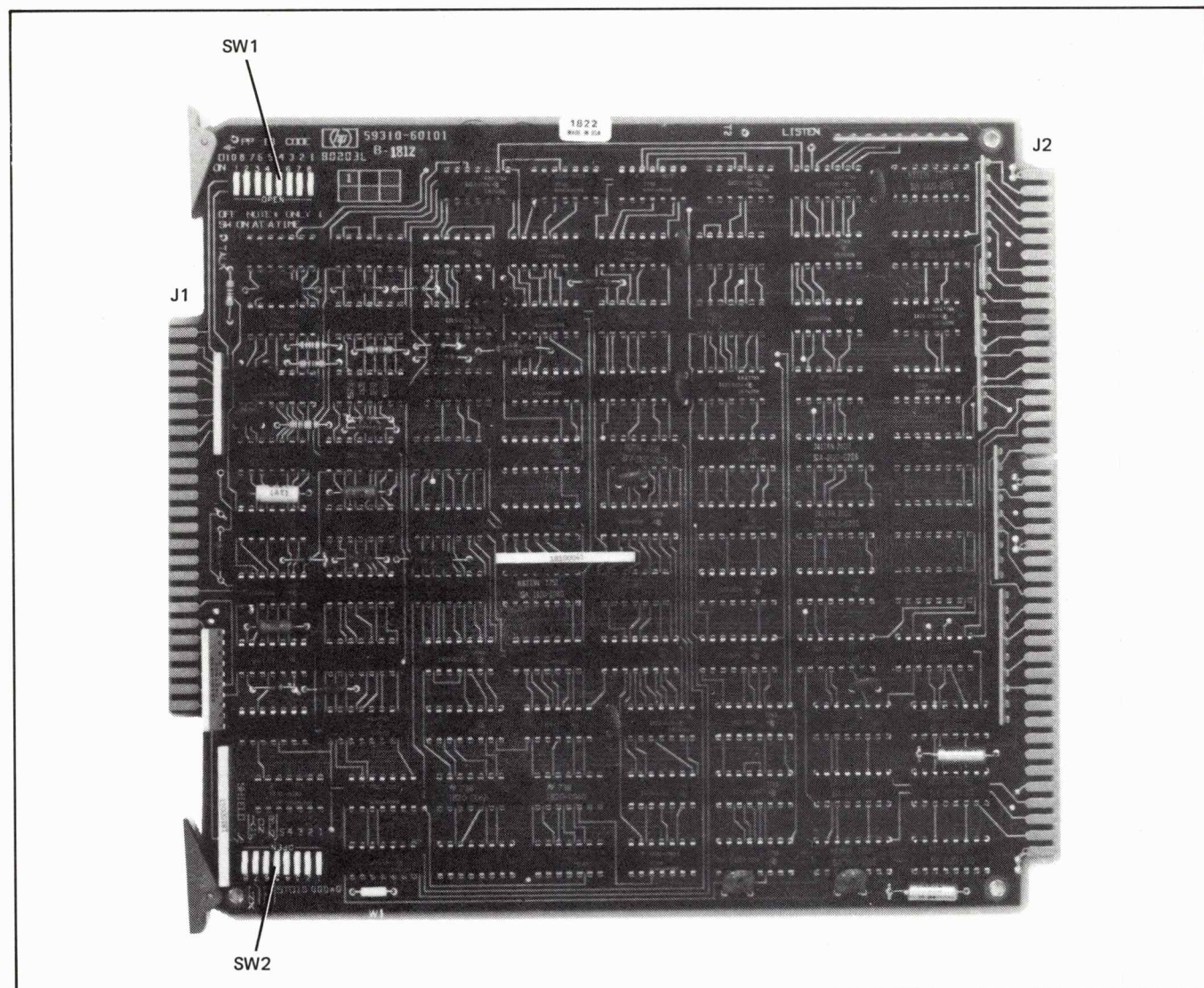
The hardwired programmable functions of the PCA are as follows:

- a. **BUS ADDRESS, 5 4 3 2 1:** Defines the lower five bits of the Talk and Listen addresses that the PCA will recognize as its own. The value set on the switches of DIP switch 2 must be between 00 000 (0₈) and 11 110 (36₈). Address 37₈ is reserved for the Unlisten and Untalk addresses.
- b. **REN:** When ON, enables the PCA to drive the BUS signal line REN. When OFF, disables the PCA from driving the BUS signal line REN. (Located on DIP switch 2.)
- c. **IFC:** When the switch is set to ON, enables the PCA to drive the BUS signal line IFC. When the switch is set to OFF, disables the PCA from driving the BUS signal line IFC. (Located on DIP switch 2.)
- d. **SHIELD:** When the switch is set to CNX, connects the shield in the bus cable to the logic circuit common. When the switch is set to DNX, disconnects the shield in the bus cable from the PCA's common. (Unless some other device connects the shield it will remain disconnected.) (Located on DIP switch 2.)
- e. **PP ID CODE:** Defines the code that the PCA will send in response to a Parallel Poll. Setting the switch to ON will cause the PCA to use the DIO signal line specified to be used. (Located on DIP switch 1.)

2-8. DIP SWITCHES

There are two DIP switches located in the upper left and lower left of the printed circuit board. See figure 2-1.

The upper left hand location (SW1) defines the identification code to be used by the card in response to a parallel poll. The lower left hand location (SW2) defines the BUS ADDRESS, REN and IFC enables, and the SHIELD connection.



7700-174

Figure 2-1. Installation Information

Select the switch positions of each DIP switch according to the functions desired as described in paragraph 2-7. The arrows associated with the labeling on the printed circuit board indicate which side of the rocker is to be depressed to cause the indicated effect. A closed switch is logical 0 and an open switch is logical 1.

2-9. STANDARD MODE OF OPERATION

The normal use of the Bus I/O PCA is the System Controller function. This requires the switches to be set.

Set DIP switch 1 (upper left) as follows:

- a. PP ID CODE: to all OFF

Set DIP switch 2 (lower left) as follows:

- a. BUS ADDRESS: sw no. 5 4 3 2 1
state 1 0 0 0 0 (20₈)
- b. REN (sw. no. 6): to ON
- c. IFC (sw. no. 7): to ON
- d. SHIELD (sw. no. 8): to CNX

NOTE

The BUS ADDRESS may be set to any value between 00 000 (0₈) and 11 110 (36₈). The value 20 is the preferred address for the computer when it is used as the system controller.

2-10. INSTALLING PRINTED CIRCUIT BOARD IN THE COMPUTER

After having selected hardwired options, the BUS I/O PCA may then be installed in the computer as follows:

- a. Set the computer's power to OFF.
- b. Insert the PCA into one of the available I/O slots of the computer. (Since the location and position will vary depending on the model of computer, refer to the computer manual for details.)

2-11. PERFORMANCE CHECK

To verify proper operation of the BUS I/O Interface run the diagnostic program as described in the *59310A/B Bus Input/Output Card Diagnostic Manual* (part no. 59310-90061).

2-12. INTERCONNECTING CABLES

Supplied with the BUS I/O Kit is a 4 metre cable (59310-60002) which contains a printed circuit board edge con-

ductor at one end and a piggy-back connector at the other end. The printed circuit board edge connector end is connected to the BUS I/O PCA J1. The end of the connector opposite from the cable must be installed so it is closest to the extractor labeled "BUS INPUT/OUTPUT".

The piggy-back connector end is connected to the peripheral device. Other devices may be added to the bus by use of the standard bus cable (not supplied), listed in table 2-2.

Table 2-2. Bus Cables

LENGTH	ACCESSORY NUMBER
1 metre	10631A
2 metres	10631B
4 metres	10631C
0.5 metres	10631D

2-13. CABLING LENGTH RESTRICTIONS

In order to ensure proper operation of the bus, two rules must be observed regarding the total *length* of bus cables when they are connected together. These are:

- a. The total length of cable permitted to be used with one Bus I/O PCA must be less than or equal to two metres times the number of devices connected together. (The Bus I/O PCA is counted as one device.)
- b. The total maximum length of cable must not exceed 20 metres.

Rule (a.) implies that there may be up to 4 metres of cable between the first two devices ($2 \text{ units} \times 2 \text{ m./device} = 4 \text{ m.}$). Additional units may be added using 2 metre cables up to a total of 10 units ($10 \text{ units} \times 2 \text{ m./device} = 20 \text{ metres}$); e.g., using one 4-metre and eight 2-metre cables ($4 + (8 \times 2) = 20$). If more than ten devices are to be connected together, cables shorter than two metres must be used between some of the devices. For example, 15 devices can be connected together using one 4-metre and thirteen one-metre cables $4 + (13 \times 1) = 17$. Other combinations may be used as long as both of the requirements of rule (a.) and (b.) are met. In making calculations, remember to count the Bus I/O PCA as one device.

2-14. CABLING CONFIGURATIONS

There are no restrictions to the ways cables may be connected together. However, it is recommended that no more than 3 to 4 piggy-back connectors be stacked together on one device. The resulting structure can exert great force on the panels of the device where the connector is mounted and could cause mechanical damage.

The configuration may be linear (all cables connected end to end) or in a star (all cables branching out from a central point) or any combination of the above.

OPERATION AND PROGRAMMING

SECTION

III

3-1. INTRODUCTION

This section explains the operation and programming of the 59310B Bus I/O PCA (Printed Circuit Assembly) in table 3-1.

3-2. HP INTERFACE (HP-IB) BUS LINES

The HP-IB has 24 lines with 16 signals. The bus lines and changes are listed in table 3-1.

Table 3-1. Bus Line Nomenclature

ABBREVIATION	NAME	ABBREVIATION	NAME
DIO1	Data Input Output 1 thru 8	NRFD	Not Ready for Data
DIO2		NDAC	Not Data Accepted
DIO3			
DIO4		IFC	Interface Clear
DIO5			
DIO6			
DIO7			
DIO8			
DAV	Data Valid	SRQ	Service Request
		ATN	Attention
		EIO	End or Identify
		REN	Remote Enable
			Common (Ground)

3-3. BUS FUNCTIONS AVAILABLE TO THE COMPUTER

Several functions on the HP-IB are usable by the computer. These functions are described in the following paragraphs.

3-4. LISTEN FUNCTIONS

The computer can input data from the bus when addressed. The listen functions include the following capabilities.

Addressable Listen: The PCA becomes addressed to Listen when a controller sends its Listen Address.

Programmable Listen: The PCA becomes addressed to Listen by the computer via software control.

End of Record Detection: An End of Record (EOR) Flag will be set if the card is addressed to Listen and is receiving data and the EOI line goes "low". In addition, if enabled by software control, an ASCII Line Feed (012₈) on the data lines will also set the EOR Flag. The EOR Flag can be tested by software or used to generate an interrupt.

Service Requesting: If enabled by software control and not addressed to Listen and ready to receive data, the PCA will generate a Service Request (SRQ).

3-5. TALK FUNCTIONS

The computer can output data to the bus when addressed. The talk functions include the following capabilities:

Addressable Talk: The PCA becomes addressed to Talk when a controller sends its Talk Address.

Programmable Talk: The PCA becomes addressed to Talk by the computer via software control.

End of Record Signaling: The computer can set EOI Low with the last byte or after the last byte indicating that End of Record has occurred. If enabled by program control, EOI will be set Low if an ASCII Line Feed (012₈) is output.

Service Requesting: If enabled by software control and not addressed to talk and ready to send data, the Bus I/O PCA will generate a Service Request (SRQ).

Serial Poll Identification: Allows the computer to respond to a controller making a serial poll. The controller sending the "serial poll enable" command will set the "serial poll mode" flag which may be tested via software or used to cause an interrupt. The computer may then send its status byte to the controller when addressed to Talk.

3-6. CONTROLLER FUNCTIONS

The computer can manage the activities on the bus by sending addresses and universal commands. The computer can only perform this role if its active status is set. (A controller becomes "active" if designated by another controller or if a system controller and it activates itself.) The controller functions include the following capabilities:

Addressing and Universal Commands: The computer sets ATN Low via program control and sends address or commands to devices in the bus.

Service Request Processing: The computer can monitor for the Service Request (SRQ) line or enable it to cause an interrupt to determine if a device on the bus is requesting service.

Serial Polling: Allows the computer to determine the device(s) that have caused a Service Request. A serial poll is executed via software by sending universal commands and addresses and using the Listen Mode.

Parallel Polling: Allows the computer to determine the device(s) needing service by sending one universal command to all devices and reading the status bits returned on the data lines. If jumper W1 is installed a Parallel Poll response causes a computer interrupt.

3-7. SYSTEM CONTROLLER FUNCTIONS

The PCA as a System Controller performs all of the functions of a controller including the following additional capabilities:

Interface Clear: Allows the computer to utilize the bus or regain control by setting the bus signal line Interface Clear (IFC) "low".

Remote Enable Control: Allows the computer to enable programmable devices to switch from local to remote control by setting the bus signal line Remote Enable (REN) "low".

Automatic Activation of Controller Functions: The Bus I/O PCA automatically becomes the Active Controller when powered up or if it sets IFC "low".

3-8. COMMUNICATION FORMS BETWEEN THE I/O PCA AND COMPUTER

The information that can be transferred between the computer and the Bus I/O PCA under program control takes five forms. These include four data types which can be passed between the A/B registers and the PCA's registers. They are: (1) the Control Word, which establishes the I/O card's operating mode, (2) the Status Word which provides information about the condition of the card and the Bus, (3) Output Data, which is transmitted from the computer to the bus and (4) Input Data which is received from the bus. Input Data and Output Data may also be transferred under DCPC control. These are discussed in detail in paragraphs 3-19 to 3-30.

The fifth type of communication from the PCA is the flags. There are eight flags, of which seven can be tested by program instructions and one is used with DCPC. Operation of the flags is discussed in paragraphs 3-31 to 3-40. Operations under program control are controlled by use of the various computer I/O instructions.

3-9. CONTROL WORD

The control word is a 16 bit word (see figure 3-1) which is output to the I/O PCA under program control. It is divided into three parts referred to as Group 1, 2 and 3. Group 2 is further divided into two sub-groups, Group 2A and 2B. The effect on the I/O PCA of each group is independent from the other groups. Each group may be used individually or in combinations.

3-10. FUNCTIONS AND MODES

The control word is used to select the operating modes and bus functions that the PCA is to perform.

The operating modes controllable with the control word are as follows:

1. Flag selection for interrupt or by testing with the SFS or SFC instructions
2. Packaging enable/disable
3. DCPC input or output flag selection
4. Service Request enable/disable
5. ASCII Mode enable/disable
6. Forced input of data (without a handshake cycle)
7. Initialize flags

The Bus functions controllable with the Control Word are as follows:

1. Remote/Local
2. Active/Inactive Controller Function
3. Enable talker function/disable
4. Enable listener function/disable
5. Controller functions
 - a. Data Mode/Command Mode Select
 - b. Parallel Poll

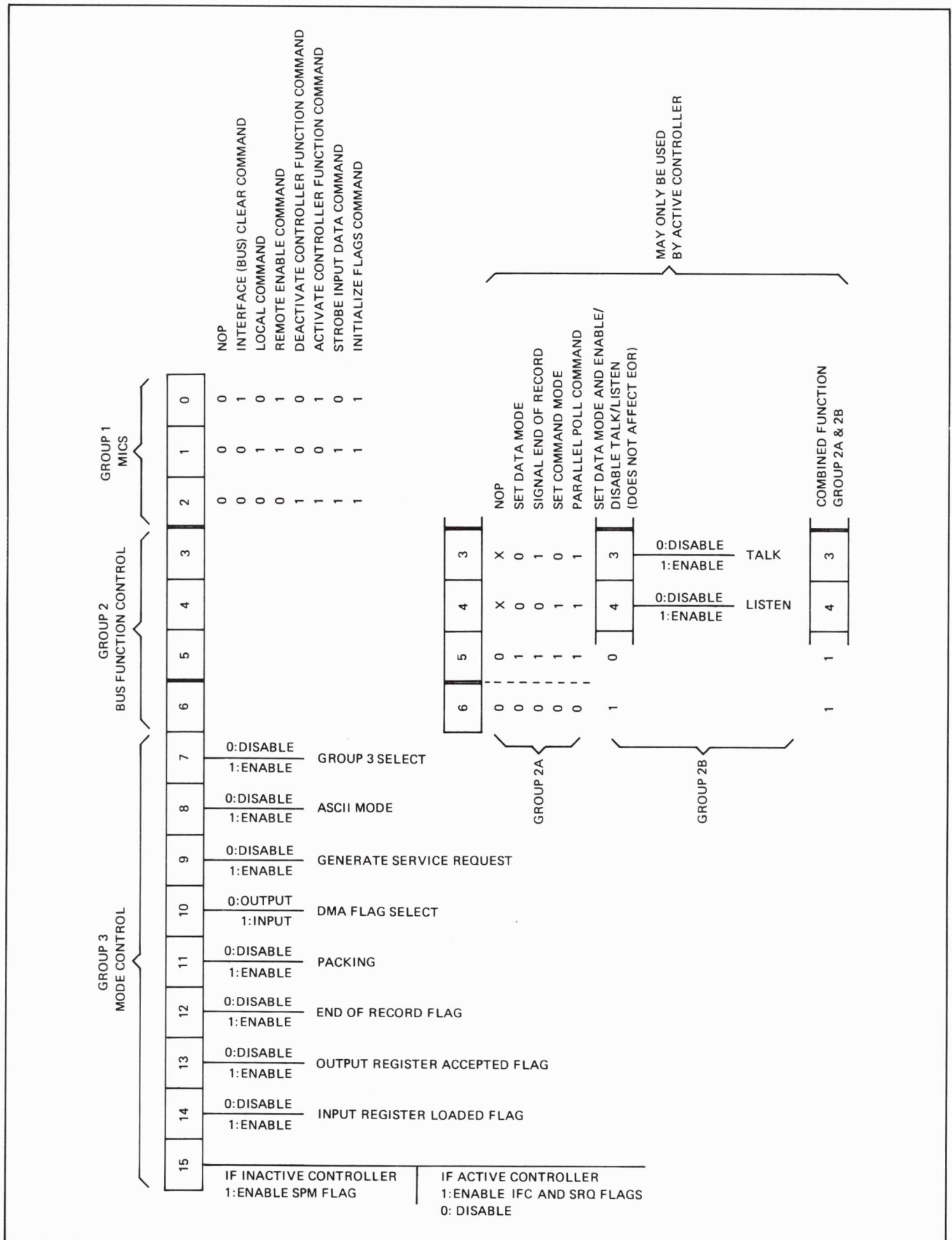


Figure 3-1. Control Word Format

3-11. OUTPUTTING THE CONTROL WORD

The control word is output to Bus I/O Interface PCA by the following sequence of instructions:

```

      .
      .
      .
      LDA   CTLWD
      STF   SC
      OTA   SC
      .
      .
      CTLWD OCT   <value>
      SC     EQU   <select code of BUS I/O card>
  
```

Do not include a NOP instruction in this program sequence as this will cause errors on the I/O bus. The value of the control word is a function of the desired operating mode of the I/O PCA and bus functions.

3-12. CONTROL WORD GROUP 1 CODING

Group 1 of the control word consists of seven coded commands using bits 0 thru 2. The commands of group 1 control the following: IFC one-shot, remote enable flip-flop, and active flip-flop. The active flip-flop forces an input cycle and initializes certain I/O control and flag flip-flops. The coding and function of each of the commands is as follows:

```

B      B
I      I
T      T
2      1      0  FUNCTION/OPERATION
  
```

0 0 0 NO OPERATION (NOP)

Does not affect the I/O PCA or the bus.

```

B      B
I      I
T      T
2      1      0  FUNCTION/OPERATION
  
```

0 0 1 INTERFACE CLEAR (IFC) COMMAND

Causes the IFC one-shot to be triggered. This sets the bus signal line IFC (Interface Clear) "low" for 100 μ sec which un-addresses all Talkers and Listeners, clears the Serial Poll Mode and deactivates all other controllers.

0 1 0 LOCAL COMMAND

Causes the remote enable flip-flop to be cleared which causes the bus signal line Remote Enable (REN) to be set high.

This causes all devices, with the possible exception of source devices (i.e., power supplies), to switch to local control, and the local lock out state to be cleared.

0 1 1 REMOTE ENABLE COMMAND

Causes the remote enable flip-flop to be set which causes the bus signal line Remote Enable (REN) to be set "low". This enables all devices on the bus to switch to remote control when addressed to Listen to their remote programming codes.

1 0 0 DEACTIVATE CONTROLLER FUNCTION COMMAND

Causes the active flip-flop to be cleared. In this state, the I/O PCA (and thus the computer) can not perform any of the functions of a controller.

1 0 1 ACTIVATE CONTROLLER FUNCTION COMMAND

Causes the active flip-flop to be set. Only if the I/O PCA is in this state may it perform the bus functions of a controller.

1 1 0 STROBE INPUT DATA COMMAND

Causes the contents of the bus data lines at the time of execution to be strobed into the input data register irrespective of the state of the handshake lines or whether the card is addressed to Listen or not. The data will go into the upper or lower half of the input data register as a function of the state of the input byte counter. The input byte counter will be toggled and the input register loaded FF set if appropriate.

1 1 1 INITIALIZE FLAGS COMMAND

Affects several flags associated with the transfer of data in and out as follows:

1. Causes the flip-flop for Output Register Loaded and Output Byte Register Loaded (ORA FF) to be cleared. This initializes the output handshake logic for subsequent output operations and/or terminates an output cycle in progress.
2. Initialized the output byte counter to byte 0 (upper half) so that data output using packing always starts with the upper half word.
3. Causes the DCPC output request flip-flop to be set so that the first DCPC Output cycle will be requested when DCPC is enabled.

4. Causes the "ready for data" flip-flop to be cleared which will set the bus signal line NRFD (Not Ready for Data) "low" if the card is addressed to Listen. This indicates to the Talker device that the card is not able to accept data yet.

3-13. CONTROL WORD GROUP 2 CODING

Group 2 of the Control Word consists of two sub-groups which control two functions each using bits 3 through 6. Group 2A is used to control the controller functions and Group 2B to control the talker/listener functions. The two sub-groups may be used independently or in combination. Bits 4 and 5 are used to select Groups 2A and 2B respectively and bits 3 and 4 to control the functions of each sub-group. Group 2 coding and functions are as follows:

B I T	B I T			
6	5	4	3	FUNCTION/OPERATION
0	0	X	X	NO OPERATION (NOP)
				Does not affect the I/O PCA or the bus.
0	1	—	—	GROUP 2A FUNCTIONS
				Accesses ATN and EOI FF's.
0	1	0	0	SET DATA MODE
				Causes the ATN (Attention) and the EOI (End of Identify) Flip-Flops to be cleared which puts the bus into the data mode so that the Talker and Listener(s) may transmit data.
0	1	0	1	SIGNAL END OF RECORD
				Clears the ATN and sets the EOI Flip-Flops which sets the bus signal line EOI (End or Identify) "low" if addressed to Talk. This indicates that the next byte sent as a Talker is the last in the string.
0	1	1	0	SET COMMAND MODE
				Sets the ATN and clears the EOI Flip-Flops which sets the Bus signal line ATN "low" and EOI "high". This puts the bus into the command mode which enables the computer to send commands and addresses.

0	1	1	1	PARALLEL POLL COMMAND
				Sets the ATN and EOI flip-flops which sets the bus signal lines ATN and EOI "low". This initiates a parallel poll. Devices so equipped, respond on a preassigned data line.
B I T	B I T			
6	5	4	3	FUNCTION/OPERATION
1	0	—	—	GROUP 2B FUNCTIONS
				Accesses Talk and Listen flip-flops. All Group 2B codes cause the data mode to be set simultaneously (i.e., the ATN FF is cleared).
1	0	0	0	DISABLE LISTEN AND DISABLE TALK FUNCTIONS
				Clears both the Talk and Listen flip-flops which prevents the I/O PCA from transmitting or receiving data.
1	0	0	1	DISABLE LISTEN AND ENABLE TALK FUNCTIONS
				Clears the Listen flip-flop and sets the Talk flip-flop, thereby enabling the PCA to send data to the bus.
1	0	1	0	ENABLE LISTEN AND DISABLE TALK FUNCTIONS
				Sets the Listen flip-flop and clears the Talk flip-flop, thereby enabling the PCA to receive data from the bus.
1	0	1	1	ENABLE LISTEN AND ENABLE TALK
				Sets both the Talk and Listen flip-flops, allowing the PCA to send data to itself. This is generally useful only for diagnostic purposes.
1	1	—	—	COMBINED ACTION OF GROUPS 2A & 2B
				Both the functions indicated by bit 3 and 4 in Groups 2A and 2B will be performed.

3-14. CONTROL WORD GROUP 3 CODING

Group 3 of the control word consists of eight mode control functions coded with one bit per function using bits 8 through 15. Bit 7 enables or disables the effect of the other bits in the group. Group 3 coding and functions are as follows:

Bit 7	GROUP 3 SELECT
	When Bit 7 = 1, enables bits 8 through 15 to control their specified functions.
	When Bit 7 = 0, disables bits 8 through 15 from having any effect in controlling their designated functions.
Bit 8	ASCII MODE ENABLE
	When Bit 7 = 1, enables the ASCII mode logic (see paragraph 3-122 for details of the operation of the ASCII Mode.)
	When Bit 7 = 0, disables the ASCII Mode.
Bit 9	GENERATE SERVICE REQUEST ENABLE
	When Bit 9 = 1, enables the bus I/O PCA to generate a Service Request (set the Bus signal line SRQ "low") if:
	1(a). The Talk flip-flop is clear and (b) the Output Byte Register flip-flop is set.
	2(b). The Listen flip-flop is clear and (b) the NRFD flip-flop is set.
	When bit 9 = 0, the PCA is disabled from driving the SRQ line (it is set to OFF).
Bit 10	DCPC FLAG SELECT
	Selects which flag is to be used to request a DCPC cycle.
	When Bit 10 = 0, the DCPC output request flag is selected.
	When Bit 10 = 1, the input register loaded flag is selected.

Bit 11

PACKING ENABLE

When Bit 11 = 1, enables the packing and unpacking logic for both input and output.

When Bit 11 = 0, disables the packing logic.

Bits 12-15

FLAG SOURCE SELECT

Selects which flags can be tested by the SFS or SFC instructions or can be used to cause an interrupt.

Bit 12

Enables the end-of-record flag.

Bit 13

Enables the output register accepted flag.

Bit 14

Enables the input register loaded flag.

Bit 15

If the active flip-flop is set, enables the bus clear as Service Request Flag (SRQ).

If the active flip-flop is clear, enables Serial Poll Mode Flag.

3-15. STATUS WORD

The status word is a 16 bit word (see figure 3-2) which is input under program control to obtain information about the operating conditions of the Bus I/O Interface PCA and the bus.

3-16. STATUS WORD FUNCTION

With the status word, the following can be determined:

1. Which one or more of the six flags have occurred (EOR, ORA, IRC, IFC, SRQ, SPM).
2. The states of five of the bus signal lines (REN, ATN, DAV, NRFD and NDAC).
3. Which of the three bus interface functions the I/O card is currently enabled to perform (Talk, Listen, Active Controller).
4. The highest priority response to a parallel poll.

3-17. INPUTTING THE STATUS WORD

The status word is transferred to the A or B registers of the computer using the following sequence of machine instructions:

3-18. STATUS WORD CODING

The coding of each of the bits of the status word is as follows:

or

STF	SC
LIA	SC
STF	SC
LIB	SC
SC	EQU <select code of BUS I/O card>

NOTE

A OTA/B instruction may not be executed between the STF and LIA/B or inputting of data will result.

Bits 0-3

PARALLEL POLL PRIORITY ENCODED IDENTIFICATION

Indicates the highest priority response to a parallel poll or the occurrence a "bus clear" command. Highest priority is assigned to IFC followed by DIO8, etc.

The priority encoding scheme is shown in Figure 3-2.

Bit 4

ACTIVE FLIP-FLOP STATUS

Indicates the state of the ACTIVE Flip-Flop.

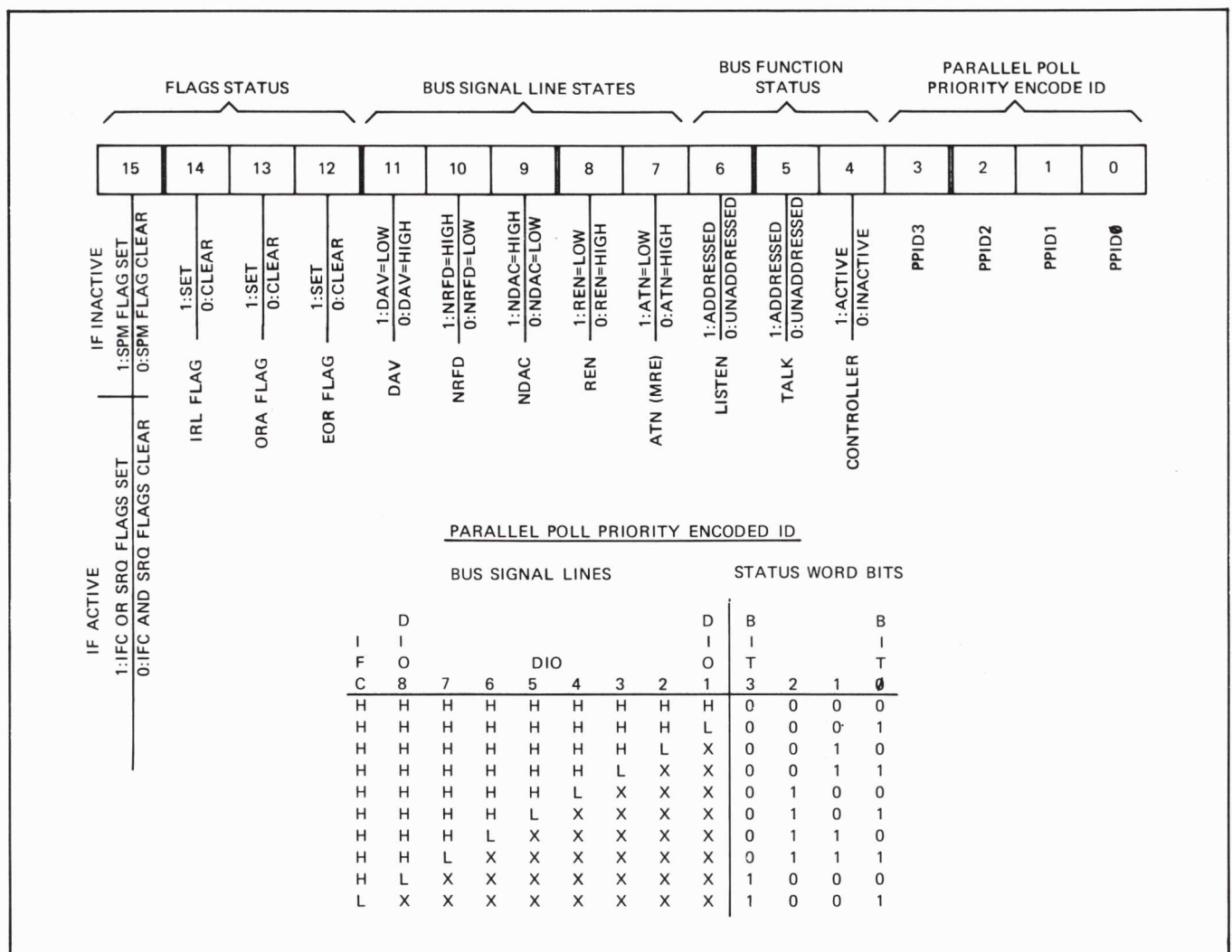


Figure 3-2. Status Word Format

	<p>If Bit 4 = 1, the ACTIVE Flip-Flop is set.</p> <p>If Bit 4 = 0, the ACTIVE Flip-Flop is reset.</p>		<p>If Bit 10 = 1, NRFD is "high".</p> <p>If Bit 10 = 0, NRFD is "low".</p>
Bit 5	<p>TALK F STATUS</p> <p>Indicates the state of the TALK Flip-Flop.</p> <p>If Bit 5 = 1, the TALK Flip-Flop is set (i.e., the PCA is addressed to talk).</p> <p>If Bit 5 = 0, the TALK Flip-Flop is reset (i.e., the PCA has not been addressed to talk).</p>	Bit 11	<p>DAV LINE STATUS</p> <p>Indicates the state of the bus signal line DAV.</p> <p>If Bit 11 = 1, DAV is "low".</p> <p>If Bit 11 = 0, DAV is "high".</p>
Bit 6	<p>LISTEN FLIP-FLOP STATUS</p> <p>Indicates the state of the LISTEN Flip-Flop.</p> <p>If Bit 6 = 1, the LISTEN Flip-Flop is set (i.e., the PCA is addressed to listen).</p> <p>If Bit 6 = 0, the LISTEN Flip-Flop is reset (i.e., the PCA has not been addressed to listen).</p>	Bit 12	<p>END OF RECORD (EOR) FLAG STATUS</p> <p>Indicates the state of the End of Record Flag.</p> <p>If Bit 12 = 1, EOR FLG has been set.</p> <p>If Bit 12 = 0, EOR FLG has not been set.</p>
Bit 7	<p>ATN LINE STATUS</p> <p>Indicates the state of the bus signal line ATN.</p> <p>If Bit 7 = 1, ATN is "low". (bus in Command Mode).</p> <p>If Bit 7 = 0, ATN is "high". (bus in Data Mode)</p>	Bit 13	<p>OUTPUT REGISTER ACCEPT (ORA) FLAG</p> <p>Indicates the state of the ORA Flag.</p> <p>If Bit 13 = 1, the ORA Flag has been set.</p> <p>If Bit 13 = 0, the ORA Flag is clear.</p>
Bit 8	<p>REN LINE STATUS</p> <p>Indicates the state of the bus signal line REN.</p> <p>If Bit 8 = 1, REN is "low". (bus is Remote Enabled).</p> <p>If Bit 8 = 0, REN is "high". (bus is in Local).</p>	Bit 14	<p>INPUT REGISTER LOADED (IRL) FLAG</p> <p>Indicates the state of the IRL Flag.</p> <p>If Bit 14 = 1, the IRL Flag has been set.</p> <p>If Bit 14 = 0, the IRL Flag is clear.</p>
Bit 9	<p>NDAC LINE STATUS</p> <p>Indicates the state of the bus signal line NDAC.</p>	Bit 15	<p>INTERFACE CLEAR (IFC), SERVICE REQUEST (SRQ) AND SERIAL POLL MODE (SPM) FLAG STATUS</p> <p>If Active (Bit 4 = 1), Bit 15 = 1 indicates that either the IFC or SRQ Flags have been set and Bit 15 = 0 indicates that both the IFC and SRQ Flags are clear.</p>
Bit 10	<p>NRFD LINE STATUS</p> <p>Indicates the state of the bus signal line NFRD.</p>		<p>If Inactive (Bit 4 = 0), Bit 15 = 1 indicates that the SPM Flag has been set and Bit 15 = 0 indicates that the SPM Flag is clear.</p>

3-19. DATA OUTPUT

3-20. DATA TRANSFER CAPABILITIES

Data can be transferred from the computer to the bus via the A or B registers under program control or via memory under DCPC (Dual Channel Port Controller) control. Either whole (16 bits) or half words (8 bits) can be output from the computer. If whole words are to be used, the I/O PCA's packing feature must be enabled by outputting a control word.

3-21. OUTPUT DATA TYPES

Data that is outputted can be classified into three types. They are distinguished by the affect they have on the devices on the bus and the I/O card. Each is output in the same manner, only their affect is different. All data type can be output with or without packing.

The function of the three data types are:

1. To send information (device data) from the computer to a device(s) on the bus while the computer is acting as the Talker. Coding and Formatting is a function of the devices.
2. To send Addresses and coded Commands to the bus while the computer is acting as the Controller. Codes are defined by bus.
3. To send ASCII data, control codes, Addresses and Commands when the I/O Card is in the ASCII Mode. Some codes are defined by I/O Card.

3-22. OUTPUT DATA REGISTERS

There are two registers on the PCA which store data received from the computer prior to being sent over the bus. These are the Output Word Register (OWR) and the Output Byte Register (OBR). The OWR is a 16 bit (2 bytes) register which stores the data received from the A or B registers or memory. The OBR is an 8 bit (1 byte) register which stores the data which is being sent via the bus.

The OWR is loaded when an OTA/B instruction is executed or simulated by DCPC. Its contents are transferred to the OBR by the I/O Card in 8 bit bytes. If packing has been enabled by outputting a control word with Bit 11 = 1, then two bytes are transferred from the OWR to the OBR for each OTA/B. If packing is disabled, only one byte is transferred for each OTA/B.

The contents of the OBR are transferred via the bus in accordance with the bus handshake lines. Each time a byte is accepted by the device(s) on the bus, a new byte is transferred from the OWR to the OBR until all the data in the OWR (one byte without packing, two with) has been accepted.

When data is being transferred under program control (using OTA/B instructions) only one or two bytes can be

stored at a time in the two registers. The acceptance of all bytes is indicated by a flag* that can be tested or used to generate an interrupt. When data is being transferred by DCPC, up to three bytes can be stored. A special flag* indicates when the OWR is empty and requests the next DCPC output cycle. This allows DCPC and bus cycles to overlap.

3-23. TO OUTPUT DATA

Data may be transferred from the A or B register of the computer to a device on the bus under program control by using the following instruction sequence:

```

      .
      .
      .
      LDA DATA
      OTA sc, C
      .
      .
      .

```

or

```

      .
      .
      .
      LDB DATA
      OTB sc, C
      .
      .
      .

```

NOTE

A STF SC instruction may not precede the LDA/B and OTA/B instructions or the data will be interpreted as a control word by the I/O card.

Data may also be transferred from the computer's memory to a device on the bus by using the DCPC option.

3-24. OUTPUT DATA FORMAT

The correspondence between the way the data appears in the A/B registers or memory and the way it appears when transferred to the bus is shown in figure 3-3.

With packing disabled, only the lower half of the machine word is transferred (bits 0-7) to the bus. The upper half (bits 8-15) is ignored. Bit 0 of the machine word corresponds to DIO1 of the bus, Bit 1 to DIO2, etc.

With packing enabled, both the upper and lower half of the machine word are transferred to the bus. The upper half is output as the first bus byte, the lower half second. Bits 0 and 7 correspond to DIO1 of the bus, Bits 1 and 8 to DIO2, etc.

*See paragraphs 3-31 to 3-38.

3-25. DATA INPUT

3-26. DATA TRANSFER CAPABILITIES

Data can be transferred from the bus to the computer's A or B registers under program control or to the computers' memory under Dual Channel Port Controller (DCPC) control. One or two bus bytes may be packed into one computer word by the I/O card, as selected by outputting a control word.

NOTE

Devices transferring data bytes to the computer under DCPC control must complete the 3-wire Handshake in less than three microseconds; otherwise each data byte will be duplicated.

3-27. INPUT DATA TYPE

The only type of data that can be input is data received from a device on the bus while the computer is addressed

to *listen* and the device to *talk*. The coding and formatting of the data is a function of the two devices.

3-28. INPUT WORD REGISTER

The Input Word Register (IWR) is a 16 bit register on the I/O card which can store one or two bytes of data received from a device on the Bus.

One byte is loaded into the IWR each time a bus handshake cycle occurs. It will be loaded with one byte if packing is disabled and two bytes if packing is enabled. When the IWR is full (1 byte without packing, 2 with) a flag* will be set which can be tested, used to cause an interrupt, or used to request a DCPC input cycle. The contents of IWR is transferred to the A or B registers when a LIA/B or MIA/B instruction is executed or to memory when a DCPC cycle simulates a LIA/B.

*See paragraphs 3-31 to 3-40.

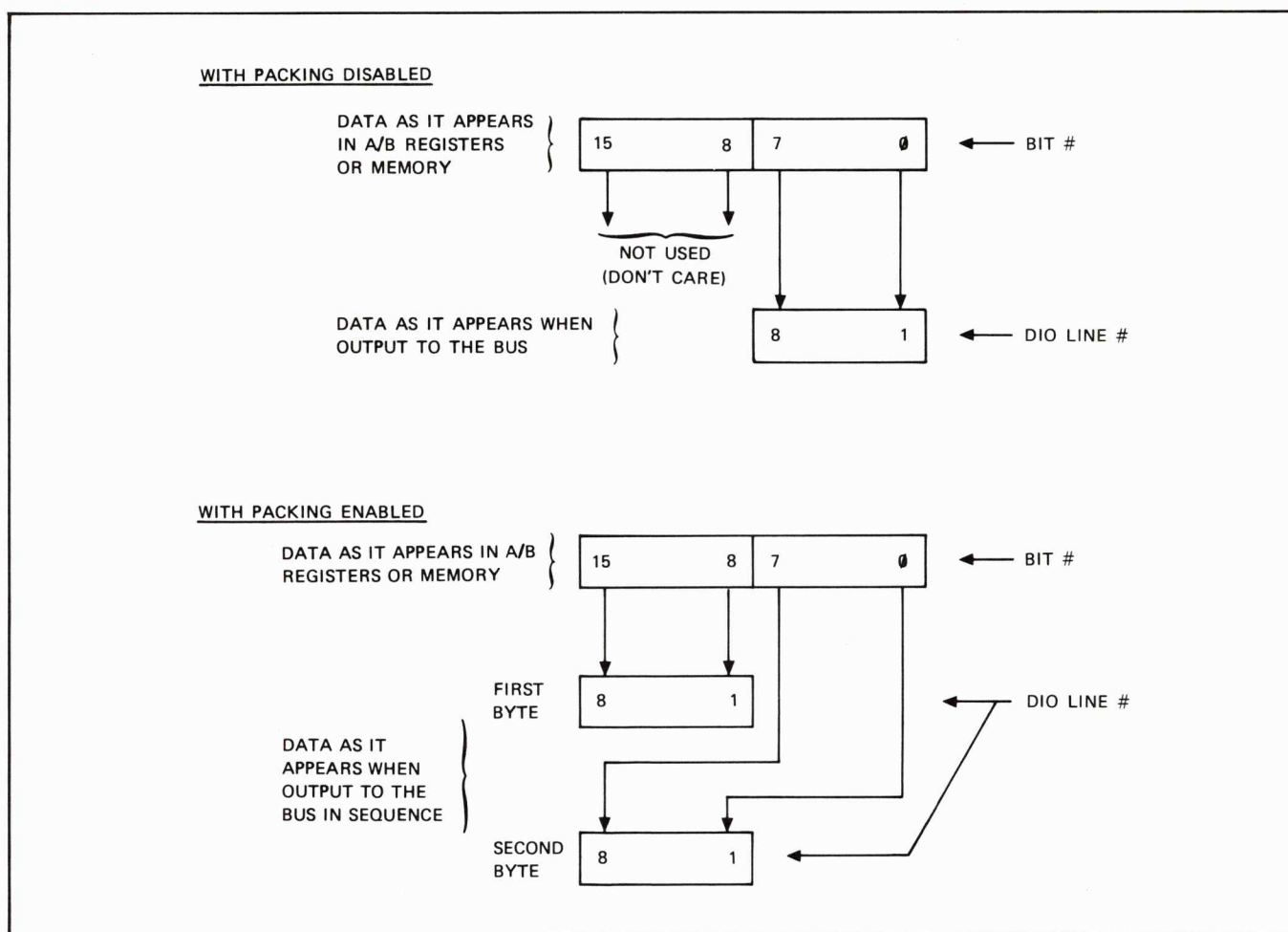


Figure 3-3. Output Data Formats

3-29. TO INPUT DATA

Data may be transferred to the A or B register under program control by the following sequence of instructions:

LIA sc, C
STA DATA

or

LIB sc, C
STB DATA

NOTE

A STF sc instruction may not precede the LIA/B instruction or the inputting of a status word will result.

Data may also be transferred to the computer's memory using the DCPC option. See paragraph 3-101.

3-30. INPUT DATA FORMAT

The correspondence between the way the data appears on the bus data lines and the way it appears when it is transferred to the A/B register or memory is shown in figure 3-4.

With packing disabled only the lower half (bits 0-7) of the computer word contains a bus byte. The upper half (bits 8-15) will contain all zeroes. The bus signal line DIO1 corresponds to Bit 0, DIO2 to Bit 1, etc.

With packing enabled both the upper and lower halves of the computer word will contain Bus bytes. The upper half will contain the first byte received, the lower the second. The bus signal line DIO1 corresponds to Bit 0 and Bit 8, DIO2 to Bits 1 and 9, etc.

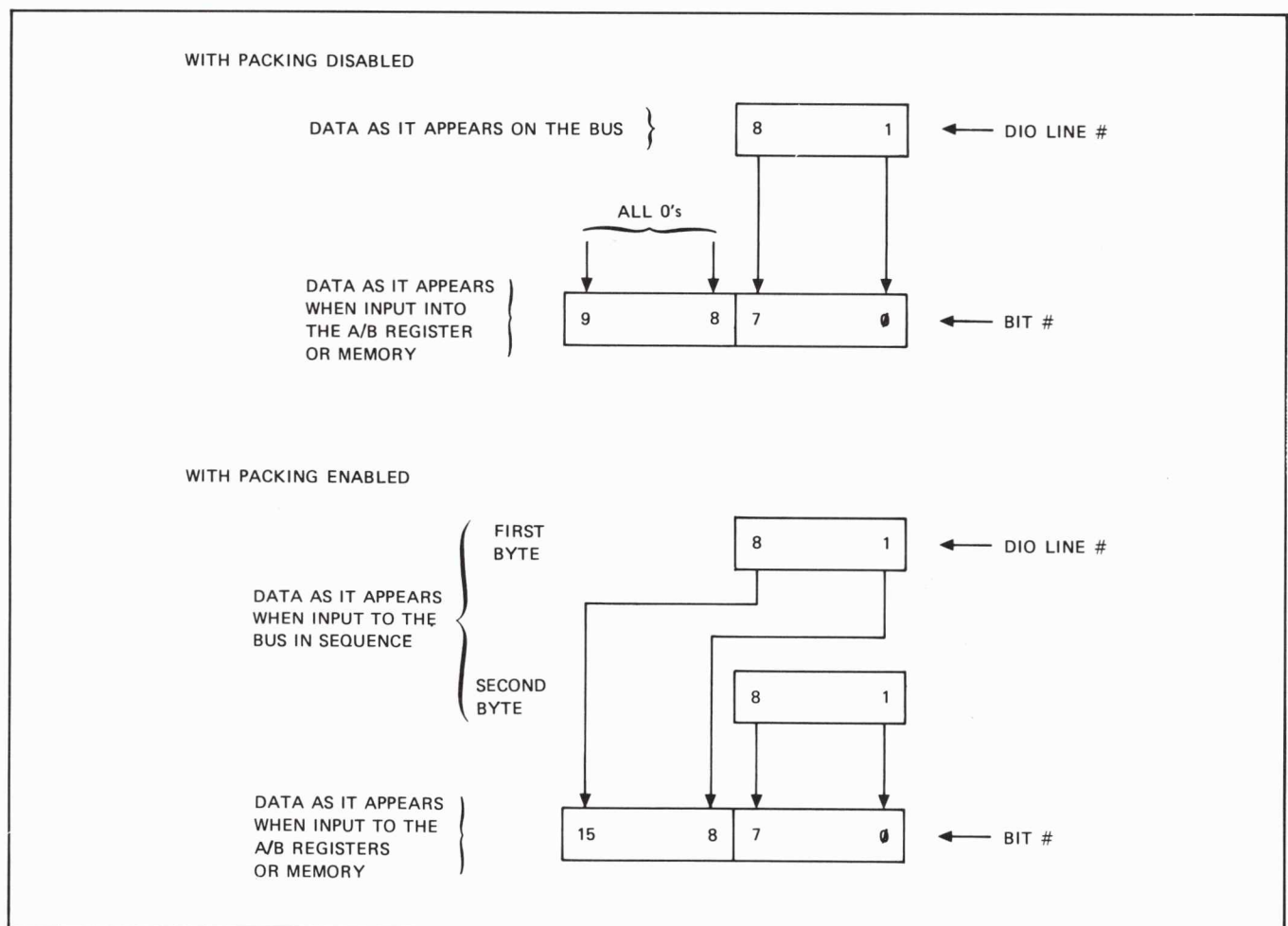


Figure 3-4. Input Data Formats

3-31. FLAGS

3-32. FLAG ORGANIZATION

There are eight flags associated with various aspects of the cards' and the bus' operation. Six of the flags (EOR, ORA, IRL, IFC, SRQ and SPM Flags) can be selectable combined to set a seventh flag (Main Flag) which can be tested by the program or used to cause an interrupt. The six flags may also be tested by inputting a status word. The eighth flag is used in conjunction with outputting data under DCPC control.

3-33. MAIN FLAG

The main flag indicates that at least one auxiliary flag has been set. It is set if any one of the auxiliary flags selected by the control word occurs. It is cleared by a CLF instruction if the control flip-flop is clear.

The state of the main flag can be tested by the SFS or SFC instructions. It may also be used to cause an interrupt if it is set and the control flip-flop is set and the interrupt system has been turned on (by a STF 0 instruction).

3-34. END OF RECORD FLAG (EOR)

The End of Record (EOR) Flag indicates that the byte of data received is the last in the string. The EOR Flag is set only if the bus I/O PCA is addressed to Listen and the talker signals "END" (EOI is low) or an ASCII linefeed character (012₈) is received and the ASCII Mode has been enabled by the control word. The EOR Flag is cleared by a CLF instruction if the control flip-flop has been cleared.

The EOR Flag may be tested by inputting a status word. If Bit 12 = 1, the EOR flag is set. The EOR flag may be enabled to set the main flag by outputting a control word with Bit 12 = 1.

3-35. OUTPUT REGISTER ACCEPTED FLAG (ORA)

The Output Register Accepted (ORA) flag indicates when set that all data in the output word and output byte register has been accepted by the device(s) on the bus. The ORA Flag will be set if:

1. The bus I/O PCA is addressed to Talk and the bus is in the Data Mode or
2. If the bus I/O PCA is the Active Controller and the bus is in the command mode and the last byte in the OWR and OBR has been accepted.

The ORA Flag is cleared by a OTA/B instruction. It can be initially cleared by outputting a Control Word = XXXXX7₈.

3-36. INPUT REGISTER LOADED FLAG (IRL)

The Input Register Loaded (IRL) flag indicates when set that data has been loaded into the input register and is ready to be input into the computer.

The IRL Flag will be set if the I/O card is addressed to Listen and the bus is in the data mode and a handshake cycle occurs. If the packing mode is disabled, the IRL Flag will be set each time a handshake cycle occurs. If the packing mode is enabled, the IRL flag will only be set every other time a handshake cycle occurs. The IRL flag is cleared by a LIA/B or MIA/B instruction.

The IRL flag can be tested by inputting the status word and testing bit 14 or it can be used to set the main flag by outputting a control word with bit 14 = 1 or it can be selected to request DCPC cycles by outputting a control word with bit 10 = 0.

3-37. INTERFACE CLEAR FLAG (IFC)

The Interface Clear Flag (IFC) indicates when set that an interface clear command has occurred on the bus (it may or may not have been generated by the bus I/O PCA). The IFC flag is cleared by a CLF instruction if the control flip-flop is clear.

The IFC Flag can be tested by inputting a Status Word. If the Status word = X XXX XXX XX1 (0001₈), then the IFC Flag is set. It may also be enabled to set the Main Flag if the I/O card is Active by outputting a Control Word with Bit 15 = 1.

NOTE

This will also enable the SRQ Flag to set the Main Flag.

3-38. SERVICE REQUEST FLAG (SRQ)

The Service Request (SRQ) flag indicates that some device on the bus wants service from the controller. The SRQ flag is set when the first device requests service. It will remain set as long as at least one device still requires service. The SRQ flag is cleared by executing a serial poll to all devices.

The SRQ flag may be tested only if the PCA is active by inputting a status word. If Bit 15 = 1 (and Bit 4 = 1) and Bits 0-3 = 11₈, then the SRQ flag is set. If the computer is the system controller and is not executing an interface clear command, then Bits 0 - 3 need not be tested. The SRQ flag may also be enabled to set the main flag if the PCA is active and a control word with Bit 15 = 1 is output. (Note: This also enables the IFC Flag to set the main flag.)

3-39. SERIAL POLL MODE FLAG (SPM)

The Serial Poll Mode (SPM) flag indicates when set that another controller has entered the serial poll mode to determine the source of a service request. The SPM flag

will be set when the controller sends the serial poll mode enable command. It will be cleared by the controller sending the serial poll disable command or the interface clear command.

The SPM flag may be tested only if the PCA is inactive as a controller and a status word is input. If Bit 15 = 1 (and Bit 4 = 0)*, the SPM flag is set. The SPM flag can also be used to set the main flag if the PCA is inactive by outputting a control word with Bit 15 = 1.

3-40. DCPC OUTPUT REQUEST FLAG

The DCPC output request flag indicates when set that all the data in the output word register has been transferred to the output byte register. It is set at the same time the last byte is loaded into the OBR. This occurs when the previous byte has been accepted from the OBR by the device(s) on the bus. If packing is used, the DCPC output request flag will be set as the second byte is loaded. If packing is not enabled, it will be set for each byte transferred. The DCPC output request flag is cleared by a CLF instruction (during DCPC operation, it is issued by DCPC).

The DCPC output request flag can only be used to request DCPC cycles. It must be enabled to do so by outputting a control word with Bit 10 = 1. Furthermore, DCPC must be initialized with various parameters to operate properly.

3-41. MACHINE I/O INSTRUCTIONS OPERATION

This section describes the operation of each of the computer's I/O instructions with respect to the bus I/O PCA. It should be noted that some of them operate somewhat differently than the normal description of each indicates.

3-42. DIFFERENCE IN USE OF I/O INSTRUCTIONS

Specifically, the STF instruction is used differently to set a data type flip-flop, the OTA/B, LIA/B, MIA/B do more (STC's are not used with them), STC does less (only enabling interrupts) and the CLF instruction is qualified by the control flip-flop.

3-43. STF INSTRUCTION

A STF sc instruction prepares the bus I/O PCA indicated by sc to receive a control word or input a status word. Execution of a STF instruction changes the operation of the next OTA/B, LIA/B, MIA/B instruction on the PCA. Execution of a OTA/B, LIA/B, MIA/B instruction returns them to their normal operation.

*Optional

3-44. OTA AND OTB INSTRUCTIONS

An OTA sc or OTB sc loads the contents of the A or B registers into the output word register and clears the ORA Flag if preceded by a STF sc instruction, outputs a control word to the PCA indicated by sc.

3-45. LIA, LIB, MIA AND MIB INSTRUCTIONS

A LIA sc or LIB sc instruction transfers the contents of the input register or, if preceded by a STF sc instruction, the status word of the bus I/O PCA indicated by sc to the A or B registers. The MIA sc and MIB sc instructions operate the same except they merge (inclusion "or") the contents into A and B.

A LIA/B, MIA/B instruction clears the input register loaded flag, presets the input byte counter to byte 0 (first input) and sets the not ready for data (NRFD) flip-flop.

3-46. SFS AND SFC INSTRUCTIONS

A SFS sc (SFC sc) instruction causes the next instruction to be skipped (i.e., P + 2 is executed) if the main flag of the PCA indicated by sc is set (clear).

3-47. STC AND CLC INSTRUCTIONS

A STC sc instruction enables the bus I/O PCA by setting the control flip-flop. This causes an interrupt if the interrupt system is turned on, and any one of the six flags selected by the control word occurs. In addition, a STC sc prevents any subsequent CLF sc instructions from clearing all but the DCPC Output Request Flag.

A CLC sc instruction clears the control flip-flop and prevents the PCA from causing an interrupt. The cleared control flip-flop will enable CLF sc to clear main flag, EOR flag and IFC flag.

3-48. CLF INSTRUCTION

A CLF sc instruction clears the DCPC output request flag and if the control flip-flop is clear, it will also clear the main flag, the EOR flag and the IFC flag.

NOTE 1

A stand alone CLF sc instruction does not operate the same as a ,C appended to another I/O instruction. The stand alone CLF sc instruction executes as though it were STF sc ,C; thus, it prepares the I/O to receive a control word or send a status word. To effectively execute a stand alone CLF, use a CLC sc, C instruction.

NOTE 2

If the PCA has been placed in the control/status mode (via an STF instruction), execution of the CLC,C instruction will clear the main flag but *not* the EOR and IFC flags. A "dummy" LIA instruction should then be executed to return the PCA to the data mode.

3-49. ASCII MODE

The ASCII Mode is a special operating mode of the bus I/O PCA in which six of the functions of the control word may be controlled by outputting reserved data codes. These are listed in table 3-1. It also enables an ASCII Linefeed (012₈) character to set the End-of-Record (EOR) flag when receiving data while addressed to listen.

Table 3-1. ASCII Mode Codes

FUNCTION	DATA CODE		
	OCTAL	ASCII	TTY
INTERFACE CLEAR COMMAND	033	ESC	ESC
LOCAL COMMAND	002	STX	CTRL and B
REMOTE ENABLE COMMAND	003	ETX	CTRL and C
SET COMMAND MODE	016	SO	CTRL and N
SET DATA MODE	017	SI	CTRL and O
SIGNAL END OF RECORD	012	LF	LINE FEED

3-50. ENABLING THE ASCII MODE

The ASCII mode is enabled by outputting a control word with Bit 8 = 1 when Group 3 is enabled.

3-51. OPERATION WHEN OUTPUTTING

When the ASCII mode is enabled, any one of the functions shown in table 3-1 may be executed by outputting the indicated data code. The effect of each on the I/O on the bus is the same as outputting a control word for the same function.

When in the ASCII mode, all codes which have control functions defined (per table 3-1) will not be transmitted except for linefeed (012₈). Linefeed causes End-of-Record to be signaled and is transmitted to the Listener(s). (The PCA must be addressed to Talk.) The other ASCII mode codes cause an internal handshake to occur which operates the same as if a device had accepted the data. That is the ORA flag will be set, etc.

An ASCII mode code (except LF) can be output whether or not the card is addressed to Talk or in the command mode. All other codes must be output when appropriate, i.e., device data only when addressed to talk, address, etc. only when in the command mode.

The ASCII mode operates the same with or without packing enabled and under program or DCPC data transfer or any combination thereof.

3-52. OPERATION WHEN INPUTTING

If the I/O PCA is addressed to Listen and the ASCII mode has been enabled, an ASCII Linefeed (012₈) will cause the End-of-Record (EOR) flag to be set. The linefeed character will also be loaded into the input register. If packing is disabled, the receipt of the linefeed character will also set the Input Register Loaded (IRL) flag. If packing is enabled, the IRL flag will only be set if the linefeed was the second byte received.

4-1. INTRODUCTION

This section explains the theory of operation of the Bus Input/Output Interface. The circuit analysis presented in this section is limited to a description of a simplified block diagram and a detailed block diagram.

4-2. GENERAL THEORY

The purpose of the Bus I/O Interface is to interface the HP computer I/O backplane to the HP Interface Bus (HP-IB). This requires translation of the computer backplane logic levels to the TTL logic level used by the HP-IB. The HP Interface Bus uses 8-bit words which requires the conversion of the computer 16-bit word to two 8-bit words.

The Bus Input/Output PCA (Printed circuit Assembly) performs four major functions; computer control word processing, bus data output, computer data input, and status

information input to the computer. These four functions are controlled by the control signals applied from the computer through the I/O backplane to the control logic, see figure 4-1.

4-3. CONTROL WORD PROCESSING

The computer control word output, which is applied through the *BP data receivers* to the *control logic*, determines the operating mode of the Bus Input/Output PCA. When the control word processing function is initiated, the *control logic*, in response to the computer backplane signals, inhibits the *computer data converter logic* and the *bus data converter logic*. The *control logic*, in conjunction with the computer control word output, determines if the PCA is either a listener or talker; the state of the *ASCII logic*; and the logic state of the flag outputs to the computer.

4-4. BUS DATA OUTPUT

The PCA applies data to the bus lines (DIO1 through DIO8) when the *computer data converter logic* is enabled

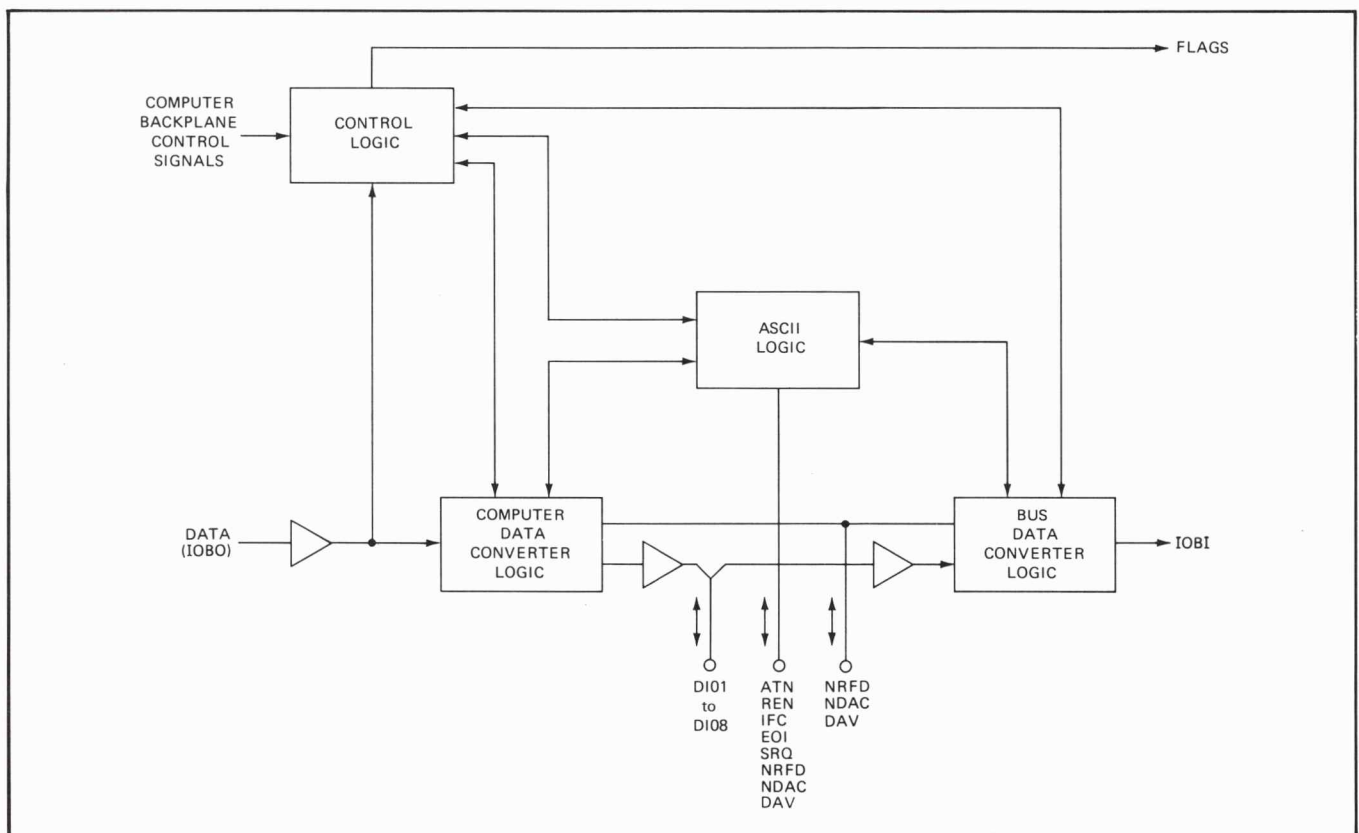


Figure 4-1. Simplified Block Diagram

by the *control logic*. The *computer data converter logic* stores the 16-bit computer word and, after the handshake sequence is completed, transfers eight bits to the bus data lines. The handshake cycle is repeated and the second eight bits are applied to the bus data lines. The data output of the *computer data converter logic* is continuously monitored by the *ASCII logic*. If the *ASCII logic* is enabled by the *control logic* and the data output is a special ASCII character, the appropriate ASCII command output is activated.

4-5. COMPUTER DATA INPUT

The Bus Input/Output card applies data to the computer when the *control logic* enables the *bus data converter logic*. The *bus data converter logic* converts two eight bit words into one 16-bit word before outputting to the computer. This is accomplished in the following manner. After the completion of the handshake cycle, the first eight bits are transferred from the bus data lines and stored in the *bus data converter logic*. The handshake cycle is repeated and the second eight bits are clocked into the appropriate output register of the *bus data converter logic*. Two eight bit words, now one 16-bit word, are clocked into the computer.

4-6. STATUS INFORMATION INPUT

The fourth major function of the PCA is the outputting of card status information to the computer. The *bus data converter logic* applies status information to the computer when the *control logic* inhibits the data output and enables the status word output. The status word output is used by the computer to monitor card operation to determine which flag caused an interrupt; to determine the state of the input/output handshake cycle; and to determine the state of the ASCII commands.

4-7. DETAILED THEORY

4-8. DATA INPUT/OUTPUT CONTROL

The four major functions of the PCA are controlled by the *data input/output control*, see figure 7-2. The *data input/output control* generates four outputs from the IOI, IOO, and STF inputs. These outputs are the IOI SC status, which puts the PCA in the computer status information function; the IOI SC data, which puts the PCA in the computer data input function; the IOO SC control, which puts the PCA in the control word processing function; and the IOO SC data, which puts the PCA in the bus data output function.

4-9. CONTROL WORD PROCESSING

4-10. WORD REGISTER AND DECODER. The computer control word determines the PCA operating mode and is processed by the *word register and decoder*. When the PCA is in the control word processing function, the transfer of data from the card to either the bus (lines

DIO1 through DIO8) or the computer is inhibited by the *data input/output control*. The control word is a 16-bit word which is divided into three functional groups; groups one, two, and three. Group one consists of bits seven through fifteen. Group two consists of bits three through six and group three consists of bits zero through two. These three groups can be used independently or in combination with each other.

The group one portion of the control word is loaded into the *word register and decoder* whenever bit seven of the control word is set high. These eight bits control the selection of which flags will cause an interrupt to be tested by a skip flag set or skip flag clear instruction. Group one also sets the ASCII mode in either the address or data mode and sets the DCPC in an input or output operation. In addition, these bits determine if the service request (SRQ) is generated on the bus with an input/output operation and if packing is enabled or disabled.

The group two portion of the control word consists of bits three through six and is subdivided into two groups: groups 2a and 2b. Group 2a controls the ATN and EOI flip-flops and is selected whenever bit five of the control word is set high. Group 2b controls the talk and listen flip-flops and is selected whenever bit six of the control word is set high. Groups 2a and 2b can be used independently or in conjunction with each other.

The third group of the control word consists of bits zero through two and is decoded by the *word register and decoder* into six control lines. These six control lines, in addition to controlling the REN and active flip-flops and the IFC single-shot, also sets the *output data control* and the *input data control* to their initial state (byte one).

4-11. EOI. The EOI flip-flop, set by the control word, determines the state of the EOI signal output line. The EOI flip-flop is reset by either the control word, an IFC signal from the bus, computer turn on, or when the computer preset push button is engaged.

4-12. REN. The REN flip-flop output is enabled when switch SW111 (position 6) is set to *REN on*. When enabled, the REN flip-flop sets the REN output line low when triggered by either the control word, the *ASCII mode logic*, computer turn on, or when the computer preset push button is pushed.

4-13. ACTIVE. The output state of the active flip-flop is controlled by the control word and the IFC single-shot. When the active flip-flop is set, the PCA becomes the bus controller. The bus controller is a device that can send out addresses and universal commands to instruments connected to the HP-IB. The active flip-flop is reset by the control word or when some other device on the bus sets IFC low.

4-14. ATN. When the active flip-flop is set, the ATN driver is enabled. This allows the ATN flip-flop to control the ATN output line. The ATN flip-flop is set by either the control word or the *ASCII mode logic*. It is reset by the

following: the control word, *ASCII mode logic*, triggering of the *IFC* single-shot, computer turn on, and when the computer preset button is pushed if the PCA is the system controller.

4-15. IFC. The *IFC* single-shot output is enabled when switch SW111 (position 7) is set to *IFC on*. In this position, the *IFC* single-shot produces a 100 microsecond pulse output when triggered by one of the following: an octal one in the lower octal digit of the control word, the *ASCII mode logic*, computer turn-on, or when the computer preset push button is pushed.

4-16. IFC BUFFER AND FILTER. The *IFC* buffer and filter, in addition to buffering the *IFC* signal line from the bus, also filters the *IFC* line. Filtering is required to eliminate fast transient noise spikes on the bus *IFC* line to prevent falsely clearing of various flip-flops.

4-17. IFC OFF. The *IFC* off flip-flop, set whenever the *IFC* bus signal line goes low, is used to generate an interrupt output to the computer. It can be tested by either a skip flag set instruction or by loading the status word into the computer. A clear flag instruction resets the *IFC* flip-flop.

4-18. BUS DATA OUTPUT.

The transfer of data from the computer to the PCA to the bus data lines uses a series of circuits on the PCA. These circuits are the *BP* data receivers, the data input/output control, the output word register, the output data control, the output handshake logic, the output byte register, and the *DIO* drivers.

4-19. BP DATA RECEIVERS. The *BP* data receivers provide signal buffering from the computer IOBO data bus to the PCA internal bus. In addition, the *BP* data receivers translate the computer backplane logic level to the TTL logic level required by the Bus Input/Output card. The output of the *BP* data receivers is applied to the word register and decoder and to the output word register.

4-20. OUTPUT WORD REGISTER. The output word register is a 16-bit register which is used to store the input data because the computer applies data to the IOBO lines for only 400 nanoseconds. Data is strobed into the output word register by the IOO SC data signal output of the data input/output control. The transfer of information from the output word register to the output byte register is controlled by the output data control and the output handshake logic.

4-21. OUTPUT BYTE REGISTER. The output byte register is an eight bit register used to transfer the data from the output word register to the *DIO* drivers in eight bit segments. This operation is controlled by two inputs applied from the output data control. One input is the word shift (ws), determining which eight bits of the output word register are applied to the *DIO* drivers. The remaining input is the clock and is used to transfer data into the output byte register.

4-22. OUTPUT DATA CONTROL. The output data control consists of a series of flip-flops. These flip-flops are used to control the output byte register, to generate a DCPC flag output, to enable the output handshake logic, and to inform the computer of the output byte register operating state. The IOO SC data signal input sets the output word register loaded flag (ORA FLG) low and, after a 100 nanosecond delay, clocks data into the output byte register. If packing is enabled, which is the ability to convert the computer 16-bit word into two eight bit words, and the output data control is in byte one, bits zero through seven are transferred to the output byte register. After the handshake cycle, the DCPC flag output is set high and the output data control is set to byte two. The DCPC flag output requests the next DCPC cycle of the computer. The second eight bits of the computer word, bits eight through fifteen, are clocked into the output byte register and applied through the *DIO* drivers to the bus output lines. After the handshake cycle, the ORA FLG output is set high, indicating to the computer that the device on the bus has accepted both eight bit words. The output data control is reset to byte one.

4-23. OUTPUT HANDSHAKE LOGIC. The output handshake logic consists of a combination of logic functions that are used to control the inputting of data to the required handshake sequence. There is a 500 nanosecond delay incorporated in the output handshake logic. After an initial 200 nanosecond delay, an enable is applied to the *ASCII mode logic*. An additional 300 nanoseconds later, if the NRFD on the bus is high, the DAV bus output line is set low. When the device on the bus has accepted the data, the DAC bus input is set high which resets the DAV output to high.

4-24. ASCII MODE LOGIC. The data output of the output byte register is also applied to the *ASCII mode logic*. If the *ASCII mode logic* is enabled, bit-8 of the control word set high, and the data is a reserved ASCII character, a low output is applied to the output handshake logic. This ends the handshake cycle, giving the appearance that the device on the bus has accepted the data. In addition, the reserved ASCII characters are decoded by the *ASCII mode logic*, determining the state of the REN flip-flop, the ATN flip-flop, or the triggering of the *IFC* single-shot.

4-25. DIO DRIVERS. The output of the output byte register is applied to the *DIO* drivers. The *DIO* drivers provide the drive for the bus data lines. These are tristate drivers and they are enabled only when the PCA is either addressed to talk or is an active controller with ATN set low.

4-26. COMPUTER DATA INPUT

The third major function of the PCA is the transferring of data from the input data and status word multiplexer to the computer. This is controlled by the input handshake logic, the input data control, and the input data/word register. The input data is applied through the *DIO* receivers to the input data/word register. The strobing of data into the input data/word register is controlled by the hand-

shake lines (DAV, NDAC, and NRFD) and the listen flip-flop. The listen flip-flop is part of the *bus communicator logic*. If the listen flip-flop is set and DAV goes low, the card can accept data into the *input data/word register*. This is controlled by the *input handshake logic*.

4-27. INPUT HANDSHAKE LOGIC. The *input handshake logic* consists of a combination of logic functions that are used to control the strobing of data into the *input data/word register*. There is a 200 nanosecond delay incorporated into the *input handshake logic*. After an initial 100 nanosecond delay, the DAV input from the bus is applied to the *input data control* and the NRFD bus output line is set high. After an additional 100 nanosecond delay, the NDAC output line is set high.

4-28. INPUT DATA CONTROL. The *input data control*, consisting of a series of flip-flops and other logic elements, provides a clock output to both the *EOR flag logic* and the upper and lower half of the *input data/word register*. Also, an input register loaded flag (IRL FLG) output is applied to the computer.

If packing is enabled, the IOI SC data output signal from the *data input/output control* sets the *input data control* to byte one. The DAV input, applied from the *input handshake logic*, results in a clock applied to the lower half of the *input data/word register*, transferring the contents of the *DIO receivers* into the *input data/word register*. The clock is also applied to the *EOR flag logic* and the *input data control* is set to byte two. The next DAV input clocks the contents of the *DIO receivers* into the upper half of the *input data/word register*. In addition, a IRL FLG is applied to the computer, indicating that the card has accepted both words of data and is ready to output.

If packing is not enabled, data is clocked into only the upper half of the *input data/word register*. The *input data control* is continuously set to byte two.

4-29. EOR FLAG LOGIC. The *EOR flag logic* will respond to the clock output from the *input data control* if enabled by either the *ASCII mode LF detector* or the *EOI flip-flop*. The EOR flag can be used to generate an interrupt and be tested by either a skip flag set instruction or by the control word.

4-30. ASCII MODE LF DETECTOR. If the *ASCII mode LF detector* is enabled by the *bus communicator logic*, it monitors the data output of the *DIO drivers*. If an octal 12 is applied to the bus data lines (DIO1 through DIO7), the *ASCII mode LF detector* will enable the *EOR flag logic*. The EOR flag logic, when clocked, will indicate end of record in the ASCII mode.

4-31. BUS COMMUNICATOR LOGIC. The *bus communicator logic*, in conjunction with the computer control word or with a bus controller, enables the PCA as either a talker or listener. The *listen flip-flop*, contained in the *bus communicator logic*, is set or reset by either the computer control word or if a controller applies the appropriate Bus Input/Output listen or un-listen address to

the data lines. Similarly, the *talk flip-flop* is set or reset by either the computer control word or if a controller applies the correct Bus Input/Output talk address to the data lines.

An additional function in the *bus communicator logic* is the *status poll flip-flop*. The *status poll flip-flop* is set when a controller applies a status poll command to the bus data lines. It is used to cause an interrupt and is tested by the skip flag set instruction. The *status poll flip-flop* enables the computer to output a status byte to the controller on request. The status poll flip-flop is reset by either the status poll disable command, generated by the controller, or when IFC is set low.

4-32. ADDRESS COMPARATOR AND ADDRESS SWITCH. Switch SW111 consists of eight, two position switches. Five of these switches, labeled *bus address* on the PCA, correspond to the *address switch*. The position of these switches determine the address of the card. The output of the *address switch* is applied to the *address comparator*. The *address comparator*, by comparing the output of the *address switch* to the data applied to the bus input data lines, determines if the PCA is addressed. When the card is addressed, the *address comparator* applies an output to the *bus communicator logic*.

4-33. SRQ REQUEST LOGIC. The *SRQ request logic* is used to generate an SRQ output, if enabled by the computer, whenever data is to be outputted or received. When enabled, an SRQ output is generated if the card is not addressed to talk and the output byte register loaded flip-flop (part of the *output data control*) is set. Also, an SRQ output is generated if the card is not addressed to listen and the ready for data flip-flop (part of the *input handshake logic*) is set.

4-34. PARALLEL POLL I.D. If a SRQ is pending, the controller may execute a parallel service request I.D. sequence by setting both ATN and EOI low. In response, the *Parallel Poll I.D.* will set the DIO line assigned to the card, line assignment is determined by the *PP I.D. code* switch SW11, low. This identifies the PCA as one of the sources of a SRQ.

4-35. PP PRIORITY AND ENCODER. The *PP priority and encoder* is used to execute a *Parallel Poll I.D.* cycle by encoding the data lines (DI01 through DI08) to the octal equivalent of the eight line code. Line DI08 has the highest priority of the data lines, octal code eight is generated if line DI08 is low. If DI08 is high, line DI07 has the highest priority. This sequence is repeated through line DI01. The IFC flip-flop generates the highest priority code, octal 11. Octal code 11 can be used to distinguish a service request from an IFC interrupt.

4-36. FLAG MULTIPLEXER and FLAGS. The *flag multiplexer* selects one of seven flag inputs that can be used as a source of interrupt. Any combination of these flags, which are enabled, will set the *flags*. The output of the *flags* is used in conjunction with the *SFS/SFC logic*,

enabling testing by these machine instructions. In addition, the *flags* output is used with the *interrupt logic* to cause an interrupt if the computer uses the interrupt system.

4-37. INTERRUPT LOGIC. The *interrupt logic* generates an interrupt output to the computer if the interrupt system in the computer is enabled and a high priority interrupt from another I/O card is not pending. If the *flags* is set, any other interrupt is locked out until the interrupt from the PCA is processed.

4-38. DCPC FLAG MULTIPLEXER. The *DCPC flag multiplexer* selects which flag, the IRL flag or the

DMA output request flag, is used to generate a DCPC service request. The control word determines flag selection.

4-39. STATUS INFORMATION INPUT

The fourth major function of the Bus Input/Output card is the transfer of the status word from the *input data and status word multiplexer* to the computer. The *data input/output control* IOI SC status output inhibits bus data transfer and enables the outputting of the status word. The status word is used by the computer to monitor card operation to determine which flag caused an interrupt; to determine the state of the handshake cycle; and to determine the state of the ASCII commands.

5-1. INTRODUCTION

This section contains troubleshooting information.

5-3. TROUBLESHOOTING

Refer to the 59310B Bus Input/Output Card Diagnostic manual, part number 59310-90061; for diagnostic program use part number 59310-16001. The program is designed to rapidly confirm proper operation of the Bus I/O PCA and to assist in troubleshooting defective cards.

REPLACEABLE PARTS

SECTION

VI

6-1. INTRODUCTION

This section contains information for ordering replaceable parts. Table 6-1 gives the meanings of the abbreviations and reference designations used in the table of replaceable parts. Table 6-2 is the list of replaceable parts and is organized as follows:

1. Components in alpha-numerical order by reference designation.

2. Miscellaneous parts.

The information given for each part consists of:

1. the Hewlett-Packard part number,
2. total quantity (Qty),
3. description of the part,
4. typical manufacturer of the part in a 5-digit code, and
5. the manufacturer's number for the part.

Total quantity for each part is given only once—at the first appearance of the part number.

Table 6-3 contains the names and addresses that correspond to the manufacturers' code numbers.

6-2. ORDERING INFORMATION

To order a part listed in the Replaceable Parts table, provide the nearest Hewlett-Packard office with the following information:

1. The Hewlett-Packard part number from the Replaceable Parts table.
2. The quantity required.

To order a part not listed in the Replaceable Parts table, provide the nearest Hewlett-Packard office with the following information:

1. Model number.

Table 6-1. Reference Designations and Abbreviations

REFERENCE DESIGNATIONS

A	= assembly	E	= miscellaneous electrical part	P	= electrical connector (movable portion); plug	U	= integrated circuit; microcircuit
AT	= attenuator; isolator; termination	F	= fuse	Q	= transistor; SCR; triode thyristor	V	= electron tube
B	= fan; motor	FL	= filter	R	= resistor	VR	= voltage regulator; breakdown diode
BT	= battery	H	= hardware	RT	= thermistor	W	= cable; transmission path; wire
C	= capacitor	HY	= circulator	S	= switch	X	= socket
CP	= coupler	J	= electrical connector (stationary portion); jack	T	= transformer	Y	= crystal unit—piezo-electric
CR	= diode; diode thyristor; varactor	K	= relay	TB	= terminal board	Z	= tuned cavity; tuned circuit
DC	= directional coupler	L	= coil; inductor	TC	= thermocouple		
DL	= delay line	M	= meter	TP	= test point		
DS	= annunciator; signaling device (audible or visual); lamp; LED	MP	= miscellaneous mechanical part				

ABBREVIATIONS

A	= ampere	avg	= average	CHAN	= channel	dc	= direct current
ac	= alternating current	AWG	= American wire gauge	cm	= centimeter	deg	= degree (temperature interval or difference)
ACCESS	= accessory	BAL	= balance	CMO	= cabinet mount only		
ADJ	= adjustment	BCD	= binary coded decimal	COAX	= coaxial		
A/D	= analog-to-digital	BD	= board	COEF	= coefficient	°	= degree (plane angle)
AF	= audio frequency	BE CU	= beryllium copper	COM	= common	°C	= degree Celsius (centigrade)
AFC	= automatic frequency control	BFO	= beat frequency oscillator	COMP	= composition	°F	= degree Fahrenheit
AGC	= automatic gain control	BH	= binder head	COMPL	= complete	°K	= degree Kelvin
AL	= aluminum	BKDN	= breakdown	CONN	= connector	DEPC	= deposited carbon
ALC	= automatic level control	BP	= bandpass	CP	= cadmium plate	DET	= detector
AM	= amplitude modulation	BPF	= bandpass filter	CRT	= cathode-ray tube	diam	= diameter
AMPL	= amplifier	BRS	= brass	CTL	= complementary transistor logic	DIA	= diameter (used in parts list)
APC	= automatic phase control	BWO	= backward-wave oscillator	CW	= continuous wave	DIFF	= differential amplifier
ASSY	= assembly	CAL	= calibrate	cw	= clockwise	AMPL	= division
AUX	= auxiliary	CW	= counterclockwise	cm	= centimeter	DPDT	= double-pole, double-throw
		CER	= ceramic	D A	= digital-to-analog	DR	= drive
				dB	= decibel		
				dBm	= decibel referred to 1 mW		

Table 6-1. Reference Designations and Abbreviations (Continued)

ABBREVIATIONS

DSB	= double sideband	MFR	= manufacturer	PIV	= peak inverse voltage	TFT	= thin-film transistor
DTL	= diode transistor logic	mg	= milligram	pk	= peak	TGL	= toggle
DVM	= digital voltmeter	MHz	= megahertz	PL	= phase lock	THD	= thread
ECL	= emitter coupled logic	mH	= millihenry	PLO	= phase lock oscillator	THRU	= through
EMF	= electromotive force	mho	= mho	PM	= phase modulation	TI	= titanium
EDP	= electronic data processing	MIN	= minimum	PNP	= positive-negative-positive	TOL	= tolerance
ELECT	= electrolytic	min	= minute (time)	P/O	= part of	TRIM	= trimmer
ENCAP	= encapsulated	MINAT	= miniature	POLY	= polystyrene	TSTR	= transistor
EXT	= external	mm	= millimeter	PORC	= porcelain	TTI	= transistor-transistor logic
F	= farad	MOD	= modulator	POS	= positive; position(s) (used in parts list)	TV	= television
FET	= field-effect transistor	MOM	= momentary	POSN	= position	TVI	= television interference
F.F	= flip-flop	MOS	= metal-oxide semiconductor	POT	= potentiometer	TWT	= traveling wave tube
FH	= flat head	ms	= millisecond	p-p	= peak-to-peak	U	= micro (10 ⁻⁶) (used in parts list)
FIL. H	= fillister head	MTG	= mounting	PP	= peak-to-peak (used in parts list)	UF	= microfarad (used in parts list)
FM	= frequency modulation	MTR	= meter (indicating device)	PPM	= pulse-position modulation	UHF	= ultrahigh frequency
FP	= front panel	mV	= millivolt	PREAMPL.	= preamplifier	UNREG	= unregulated
FREQ	= frequency	mVac	= millivolt, ac	PRF	= pulse-repetition frequency	V	= volt
FXD	= fixed	mVdc	= millivolt, dc	PRR	= pulse repetition rate	VA	= voltampere
G	= gram	mVpk	= millivolt, peak	ps	= picosecond	Vac	= volts, ac
GE	= germanium	mV p-p	= millivolt, peak-to-peak	PT	= point	VAR	= variable
GHz	= gigahertz	mVrms	= millivolt, rms	PTM	= pulse-time modulation	VCO	= voltage-controlled oscillator
GL	= glass	mW	= milliwatt	PWM	= pulse-width modulation	Vdc	= volts, dc
GND	= ground(ed)	MUX	= multiplex	PWV	= peak working voltage	VDCW	= volts, dc, working (used in parts list)
H	= henry	MY	= mylar	RC	= resistance	V(F)	= volts, filtered
h	= hour	μA	= microampere	RECT	= rectifier	VFO	= variable-frequency oscillator
HET	= heterodyne	μF	= microfarad	REF	= reference	VHF	= very-high frequency
HEX	= hexagonal	μH	= microhenry	REG	= regulated	Vpk	= volts, peak
HD	= head	μmho	= micromho	REPL.	= replaceable	Vp-p	= volts, peak-to-peak
HDW	= hardware	μs	= microsecond	RF	= radio frequency	Vrms	= volts, rms
HF	= high frequency	μV	= microvolt	RFI	= radio frequency interference	VSUR	= voltage standing wave ratio
HG	= mercury	μVac	= microvolt, ac	RH	= round head; right hand	VTO	= voltage-tuned oscillator
HI	= high	μVdc	= microvolt, dc	RLC	= resistance-inductance-capacitance	VTVM	= vacuum-tube voltmeter
HIP	= Hewlett-Packard	μVpk	= microvolt, peak	RMO	= rack mount only	V(X)	= volts, switched
HPF	= high pass filter	μV p-p	= microvolt, peak-to-peak	RND	= round	W	= watt
HR	= hour (used in parts list)	μVrms	= microvolt, rms	ROM	= read-only memory	W	= with
HV	= high voltage	μW	= microwatt	R&P	= rack and panel	WIV	= working inverse voltage
H _z	= Hertz	nA	= nanoampere	RWV	= reverse working voltage	WW	= wirewound
IC	= integrated circuit	NC	= no connection	S	= scattering parameter	W O	= without
ID	= inside diameter	NE	= neon	S	= second (time)	YIG	= yttrium-iron-garnet
IF	= intermediate frequency	NEG	= negative	S-B	= second (plane angle)	Zo	= characteristic impedance
IMPG	= impregnated	nF	= nanofarad	SCR	= silicon controlled rectifier; screw		
in	= inch	NI PL	= nickel plate	SE	= selenium		
INCD	= incandescent	N/O	= normally open	SECT	= sections		
INCL.	= include(s)	NOM	= normal	SEMICON	= semiconductor		
INP	= input	NPN	= negative-positive-negative	SHF	= superhigh frequency		
INS	= insulation	NPO	= negative-positive-zero (zero temperature coefficient)	SI	= silicon		
INT	= internal	NRFR	= not recommended for field replacement	SIL	= silver		
kg	= kilogram	NSR	= not separately replaceable	SL	= slide		
kHz	= kilohertz	ns	= nanosecond	SNR	= signal-to-noise ratio		
kΩ	= kilohm	nW	= nanowatt	SPDT	= single-pole, double-throw		
kV	= kilovolt	ORD	= order by description	SPG	= spring		
lb	= pound	OD	= outside diameter	SR	= split ring		
L	= inductance	OH	= oval head	SPST	= single-pole, single-throw		
L.C.	= inductance-capacitance	OP AMPL.	= operational amplifier				
LED	= light-emitting diode	OPT	= option				
LF	= low frequency	OSC	= oscillator				
LG	= long	OX	= oxide				
LH	= left hand	oz	= ounce				
LJM	= limit	Ω	= ohm				
LJN	= linear taper (used in parts list)	P	= peak (used in parts list)				
lin	= linear	PAM	= pulse-amplitude modulation				
LK	= lock washer	PC	= printed circuit				
WASH	= low; local oscillator	PCM	= pulse-code modulation; pulse-count modulation				
LO	= logarithmic taper (used in parts list)	PDM	= pulse-duration modulation				
LOG	= logarithmic	pF	= picofarad				
log	= logarithmic	PH BRZ	= phosphor bronze				
L.P.F.	= low pass filter	PHI.	= Phillips				
L.V	= low voltage	PIN	= positive-intrinsic-negative				
m	= meter (distance)						
mA	= milliamper						
MAX	= maximum						
MΩ	= megohm						
MEG	= meg (10 ⁶) (used in parts list)						
MET FILM	= metal film						
MET OX	= metal oxide						
MF	= medium frequency; microfarad (used in parts list)						

NOTE

All abbreviations in the parts list will be in upper case.

MULTIPLIERS

Abbreviation	Prefix	Multiple
T	tera	10 ¹²
G	giga	10 ⁹
M	mega	10 ⁶
k	kilo	10 ³
da	deka	10
d	deci	10 ⁻¹
c	centi	10 ⁻²
m	milli	10 ⁻³
μ	micro	10 ⁻⁶
n	nano	10 ⁻⁹
p	pico	10 ⁻¹²
f	femto	10 ⁻¹⁵
a	atto	10 ⁻¹⁸

2. Complete serial number, including prefix
3. Description and function of the part
4. Quantity required

6-3. HP PART NUMBER ORGANIZATION

Following is a general description of the HP part number system.

6-4. COMPONENT PARTS AND MATERIALS

Generally, the prefix of HP part numbers identifies the type of device. Eight digit part numbers are used, where the four digit prefix identifies the type of component, part, or material and the four digit suffix indicates the specific type. Following is a list of some of the more commonly used prefixes for component parts. The list includes HP manufactured parts and purchased parts.

For example, 1854-0037, 1854-0221, and 1851-0192 are all NPN transistors. The first two are silicon and the last is germanium.

Commonly-Used Prefixes for Component Parts

Prefix	Component/Part/Material
0121--	Capacitors, Variable (mechanical)
0122--	Capacitors, Voltage Variable (semiconductor)
0140--	Capacitors, Fixed
0150--	Capacitors, Fixed
0160--	Capacitors, Fixed
0180--	Capacitors, Fixed Electrolytic
0330--	Insulating Materials
0340--	Insulators, Formed
0370--	Knobs, Control
0380--	Spacers and Standoffs
0410--	Crystals
0470--	Adhesives
0490--	Relays
0510--	Fasteners
0674- thru 0778-	Resistors, Fixed (non wire wound)
0811- thru 0831-	Resistors (wire wound)
1200-	Sockets for components
1205-	Heat Sinks
1250-	Connectors (RF and related parts)
1251-	Connectors (non RF and replated parts)
1410-	Bearings and Bushings
1420-	Batteries
1820-	Monolithic Digital Integrated Circuits
1826-	Monolithic Linear Integrated Circuits
1850-	Transistors, Germanium PNP
1851-	Transistors, Germanium NPN
1853-	Transistors, Silicon PNP
1854-	Transistors, Silicon NPN
1855-	Field-Effect-Transistors
1900- thru 1912-	Diodes
1920- thru 1952-	Vacuum Tubes
1990-	Semiconductor Photosensitive and Light-Emitting Diodes
3100- thru 3106-	Switches
8120-	Cables
9100-	Transformers, Coils, Chokes, Inductors, and Filters

Table 6-2. Replaceable Parts

REFERENCE DESIGNATION	HP PART NO.	QTY	DESCRIPTION	MFR CODE	MFR PART NO.
	59310-60101	1	BOARD ASSEMBLY, BUS I/O	28480	59310-60101
C1	0180-0374	2	CAPACITOR-FXD 10UF+ -10% 20VDC TA	56289	150D106X9020B2
C2	0180-0374		CAPACITOR-FXD 10UF+ -10% 20VDC TA	56289	150D106X9020B2
C3	0160-0153	2	CAPACITOR-FXD 1000PF + -10% 200WVDC POLYE	56289	292P10292
C4	0160-0155	1	CAPACITOR-FXD 3300PF + -10% 200WVDC POLYE	56289	292P33292
C5	0160-2640	1	CAPACITOR-FXD .01UF + -20% 50WVDC CER	28480	0160-2640
C6	0160-0157	1	CAPACITOR-FXD 4700F + -10% 200WVDC POLYE	56289	29P47292
C7	0160-0153		CAPACITOR-FXD 1000PF + -10% 200WVDC POLYE	56289	292P10292
C8	0160-0154		CAPACITOR-FXD 2200PF + -10% 200WVDC POLYE	56289	292P22292
C9	0160-2197	1	CAPACITOR-FXD 10PF + -5% 300WVDC MICA	28480	0160-2197
C10	0160-0154		CAPACITOR-FXD 2200PF + -10% 200WVDC POLYE	56289	292P2292
C11	0160-0945	1	CAPACITOR-FXD 910PF + -5% 100WVDC MICA	28480	0160-0945
C12	0160-2055	8	CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C13	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C14	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C15	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C16	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C17	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C18	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C19	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
CR1	1901-0040	6	DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
CR2	1901-0040		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
CR3	1901-0040		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
CR4	1901-0040		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
CR6	1901-0040		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
R1	0757-0403	7	RESISTOR 121 1% .125W F TC=0+ -100	24546	C4-1/8-TO-121R-F
R2	0757-0403		RESISTOR 121 1% .125W F TC=+ -100	24546	C4-1/8-TO-121R-F
R3	0757-0279	1	RESISTOR 3.16K 1% .125W F TC=0+ -100	24546	C4-1/8-TO-3161-F
R4	0757-0403	1	RESISTOR 121 1% .125W F TC=0+ -100	24546	C4-1/8-TO-121R-F
R5	0757-0403		RESISTOR 121 1% .125W F TC=0+ -100	24546	C4-1/8-TO-121R-F
R6	0757-0403		RESISTOR 121 1% .125W F TC=0+ -100	24546	C4-1/8-TO-121R-F
R7	0757-0438	1	RESISTOR 5.11K 1% .125W F TC=0+ -100	24546	C4-1/8-TO-5111-F
R9	0757-0403		RESISTOR 121 1% .125W F TC=0+ -100	24546	C4-1/8-TO-121R-F
R10	0757-0403		RESISTOR 121 1% .125W F TC=0+ -100	24546	C4-1/8-TO-121R-F
R12	0683-1025	2	RESISTOR 1K 5% .25W FC TC= -400/+600	01121	CB1025
R13	0683-1025		RESISTOR 1K 5% .25W FC TC= -400/+600	01121	CB1025
R14	1810-0121	5	NETWORK-RES 9-PIN-SIP .15-PIN-SPCG	28480	1810-0121
R15	1810-0121		NETWORK-RES 9-PIN-SIP .15-PIN-SPCG	28480	1810-0121
R16	1810-0121		NETWORK-RES 9-PIN-SIP .15-PIN-SPCG	28480	1810-0121
R17	1810-0121		NETWORK-RES 9-PIN-SIP .15-PIN-SPCG	28480	1810-0121
R18	1810-0041	2	NETWORK-RES 9-PIN-SIP .15-PIN-SPCG	28480	1810-0041
R19	1810-0121		NETWORK-RES 9-PIN-SIP .15-PIN-SPCG	28480	1810-0121
R20	1810-0136	2	NETWORK-RES 10-PIN-SIP .1-PIN-SPCG	28480	1810-0136
R21	1810-0136		NETWORK-RES 10-PIN-SIP .1-PIN-SPCG	28480	1810-0136
R22	1810-0041		NETWORK-RES 9-PIN-SIP .15-PIN-SPCG	28480	1810-0041
S1	3101-1983	2	SWITCH-TGL DIP ROCKER ASSEMBLY 8-1A NS	81073	76YY2078
S2	3101-1983		SWITCH-TGL DIP ROCKER ASSEMBLY 8-1A NS	81073	76YY2078

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Continued)

REFERENCE DESIGNATION	HP PART NO.	QTY	DESCRIPTION	MFR CODE	MFR PART NO.
U13	1820-0054	8	IC SN74 00 N GATE	01295	SN7400N
U14	1820-1112	7	IC SN74LS 74 N FLIP-FLOP	01295	SN74LS74N
U15	1820-1112		IC SN74LS 74 N FLIP-FLOP	01295	SN74LS74N
U16	1820-0054		IC SN74 00 N GATE	01295	SN7400N
U17	1820-0054		IC SN74 00 N GATE	01295	SN7400N
U18	1820-1080	11	IC N8T13B DRIVER	18324	N8T13B
U21	1820-1112		IC SN74LS 74 N FLIP-FLOP	01295	SN74LS74N
U22	1820-1112		IC SN74LS 74 N FLIP-FLOP	01295	SN74LS74N
U23	1820-1056	3	IC SN74 132 N SCHMITT	01295	SN74132N
U24	1820-1112		IC SN74LS 74 N FLIP-FLOP	01295	SN74LS74N
U25	1820-1112		IC SN74LS 74 N FLIP-FLOP	01295	SN74LS74N
U26	1820-0328	3	IC SN74 02 N GATE	01295	SN7402N
U27	1820-0068	7	IC SN74 10 N GATE	01295	SN7410N
U28	1820-1080		IC N8T13B DRIVER	18324	N8T13B
U31	1820-0511	6	IC SN74 08 N GATE	01295	SN7408N
U32	1820-0328		IC SN74 02 N GATE	01295	SN7402N
U33	1820-0174	2	IC SN74 04 N INV	01295	SN7404N
U34	1820-1112		IC SN74LS 74 N FLIP-FLOP	01295	SN74LS74N
U35	1820-0328		IC SN74 02 N GATE	01295	SN7402N
U36	1820-0068		IC SN74 10 N GATE	01295	SN7410N
U37	1820-1056		IC SN74 132 N SCHMITT	01295	SN74132N
U38	1820-0054		IC SN74 00 N GATE	01295	SN7400N
U41	1820-0515	1	IC MV	07263	9602PC
U42	1820-0537	1	IC SN74 13 N SCHMITT	01295	SN7413N
U43	1820-0068		IC SN74 10 N GATE	01295	SN7410N
U44	1820-0511		IC SN74 08 N GATE	01295	SN7408N
U45	1820-0539	1	IC SN74 37 N BUFFER	01295	SN7437N
U46	1820-0054		IC SN74 00 N GATE	01295	SN7400N
U47	1820-0511		IC SN74 08 N GATE	01295	SN7408N
U48	1820-0511		IC SN74 08 N GATE	01295	SN7408N
U51	1820-1084	3	IC N8T09B DRIVER	18324	N8T09B
U52	1820-0054		IC SN74 00 N GATE	01295	SN7400N
U53	1820-0069	2	IC SN74 20 N GATE	01295	SN7420N
U54	1820-0214	2	IC:TTL BCD-TO-DECIMAL DECODER	01295	SN7442N
U55	1820-0069		IC SN74 20 N GATE	01295	SN7420N
U56	1820-1100	2	IC SN74 298 N MUXR	01295	SN74298N
U57	1820-1196	2	IC SN74LS 174 N FLIP-FLOP	01295	SN74LS174N
U58	1820-1049	3	IC DM80 97N BUFFER	27014	DM8097N
U61	1820-0621	2	IC SN74 38 N BUFFER	01295	SN7438N
U62	1820-0068		IC SN74 10 N GATE	01295	SN7410N
U63	1820-1084		IC N8T09B DRIVER	18324	N8T09B
U64	1816-0188	1	IC 256-BIT ROM TTL	28480	1816-0188
U65	1820-1195	7	IC SN74LS 175 N FLIP-FLOP	01295	SN74LS175N
U66	1820-1100		IC SN74 298 N MUXR	01295	SN74298N
U67	1820-0788		IC SN74 174 N FLIP-FLOP	01295	SN74174N
U68	1820-1049		IC DM80 97N BUFFER	27014	DM8097N
U71	1820-1056		IC SN74 132 N SCHMITT	01295	SN74132N
U72	1820-1053	5	IC SN74 14 N SCHMITT	01295	SN7414N
U73	1820-1084		IC N8T09B DRIVER	18324	N8T09B
U74	1820-1080		IC N8T13B DRIVER	18324	N8T13B

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Continued)

REFERENCE DESIGNATION	HP PART NO.	QTY	DESCRIPTION	MFR CODE	MFR PART NO.
U75	1820-0084	1	IC SN74 53 N GATE	01295	SN7453N
U76	1820-1195		IC SN74LS 175 N FLIP-FLOP	01295	SN74LS175N
U77	1820-1195		IC SN74LS 175 N FLIP-FLOP	01295	SN74LS175N
U78	1820-1049		IC DM80 97N BUFFER	27014	DM8097N
U81	1820-1053		IC SN74 14 N SCHMITT	01295	SN7414N
U82	1820-0068		IC SN74 10 N GATE	01295	SN7410N
U83	1820-1053		IC SN74 14 N SCHMITT	01295	SN7414N
U84	1820-0070	2	IC SN74 30 N GATE	01295	SN7430N
U85	1820-1082	1	IC SN74 147 N ENCODER	01295	SN74147N
U86	1820-1195		IC SN74LS 175 N FLIP-FLOP	01295	SN74LS175N
U87	1820-1080		IC N8T13B DRIVER	18324	N8T13B
U88	1820-1080		IC N8T13B DRIVER	18324	N8T13B
U91	1820-0621		IC SN74 38 N BUFFER	01295	SN7438N
U93	1820-0214		IC:TTL BCD-TO-DECIMAL DECODER	01295	SN7442N
U94	1820-1053		IC SN74 14 N SCHMITT	01295	SN7414N
U95	1820-0174		IC SN74 04 N INV	01295	SN7404N
U96	1820-1195		IC SN74LS 175 N FLIP-FLOP	01295	SN74LS175N
U97	1820-1080		IC N8T13B DRIVER	18324	N8T13B
U98	1820-1080		IC N8T13B DRIVER	18324	N8T13B
U101	1820-0782	1	IC SN74 27 N GATE	01295	SN7427N
U102	1820-0511		IC SN74 08 N GATE	01295	SN7408N
U103	1820-0068		IC SN74 10 N GATE	01295	SN7410N
U104	1820-0068		IC SN74 10 N GATE	01295	SN7410N
U105	1820-1053		IC SN74 14 N SCHMITT	01295	SN7414N
U106	1820-1195		IC SN74LS 175 N FLIP-FLOP	01295	SN74LS175N
U107	1820-1080		IC N8T13B DRIVER	18324	N8T13B
U108	1820-1080		IC N8T13B DRIVER	18324	N8T13B
U112	1820-0054		IC SN74 00 N GATE	01295	SN7400N
U113	1820-0706	1	IC COMPTR	07263	9324DC
U114	1820-0070		IC SN74 30 N GATE	01295	SN7430N
U115	1820-0511		IC SN74 08 N GATE	01295	SN7408N
U116	1820-1195		IC SN74LS 175 N FLIP-FLOP	01295	SN74LS175N
U117	1820-1080		IC N8T13B DRIVER	18324	N8T13B
U118	1820-1080		IC N8T13B DRIVER	18324	N8T13B
W1	8159-0005	1	WIRE 22AWG W PVC 1X22 80C	0073G	L-2007-1
			MISCELLANEOUS PARTS		
	5040-6001	1	EXTRACTOR:PC BOARD	28480	5040-6001
	1480-0116	2	EXTRACTOR PIN:1/16" DIA	73957	GP24-063X250-12
	5040-6065	1		28480	5040-6065
	1480-0116		EXTRACTOR PIN:1/16" DIA	73957	GP24-063X250-12

See introduction to this section for ordering information

Table 6-3. Manufacturers Code List

MFR NO.	MANUFACTURER NAME	ADDRESS	ZIP CODE
01121	ALLEN BRADLEY CO	MILWAUKEE, WI	53212
01295	TEXAS INSTR INC SEMICONDUCTOR CMPNT DIV	DALLAS, TX	75231
07263	FAIRCHILD SEMICONDUCTOR DIV	MOUNTAIN VIEW, CA	94040
16299	CORNING GL WK ELEC CMPNT DIV	RALEIGH, NC	27604
18324	SIGNETICS CORP	SUNNYVALE, CA	94086
22526	BERG ELECTRONIC INC	CUMBERLAND PA	17070
24546	CORNING GLASS WORKS (BRADFORD)	BRADFORD, PA	16701
27014	NATIONAL SEMICONDUCTOR CORP	SANTA CLARA, CA	95051
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO, CA	94304
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS, MA	01247

SCHEMATIC DIAGRAMS

SECTION

VII

7-1. INTRODUCTION

This section contains information for schematic diagram notes, reference designation system, identification markings on PC board, an overall block diagram, schematic simplified logic diagram and component locator.

7-2. SCHEMATIC DIAGRAM NOTES

Figure 7-1 shows the symbols used on the schematic diagrams. Notes are also included on each schematic diagram.

7-3. IDENTIFICATION MARKINGS ON PRINTED-CIRCUIT BOARDS

HP printed circuit boards (see figure 7-1) have four identification numbers; an assembly part numbers, a date code, a revision letter, and a production code.

The assembly part number has 10 digits (such as 59310-60101) and is the primary identification. All assemblies with the same part number are interchangeable. When a production change is made on an assembly that makes it incompatible with previous assemblies, a change in part number is required. The date code (such as 1812) is used to document minor electrical changes. As changes are made, the date code is incremented. When replacement boards are ordered, you may receive a replacement with a different date code. If there is a difference between the date code

marked on the board and the schematic in this manual, a minor electrical difference exists. If it is a higher number, refer to the loose leaf manual change sheets for this manual. If the manual change sheets are missing, contact your local Hewlett-Packard Sales and Service Office. See the listing on the back cover of this manual.

Revision letters (A, B, etc.) denote changes in printed circuit layout. For example, if a capacitor type is changed (electrical value may remain the same) and requires different spacing for its leads, the printed circuit board layout is changed and the revision letter is incremented to the next letter. The production code is the four digit, seven segment number used for production purposes.

Symbols are used on PC boards to aid in identifying pin numbers, diode elements etc. as follows:

Δ OR □ IDENTIFIES: Pin 1 of dip and flat-pack IC's.
Tab of TO cases.
+ side of electrolytic capacitors.
Pin 1 of resistor packs.
Cathode of diodes.
Section 1 of dip switches.

7-4. COMPONENT LOCATORS

Figure 7-4 component locator for the printed circuit assembly is next to the schematic.

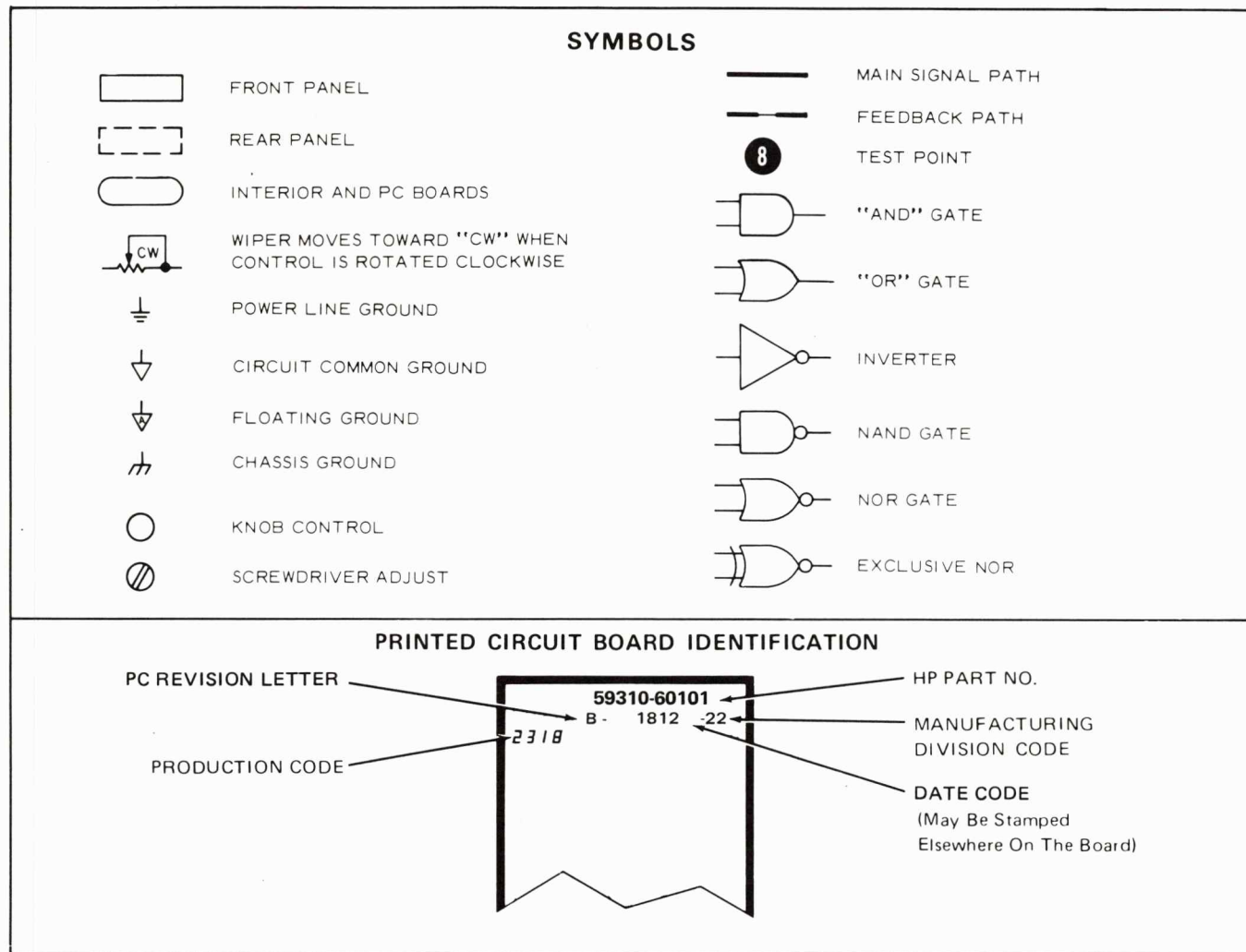


Figure 7-1. Schematic Diagram Notes

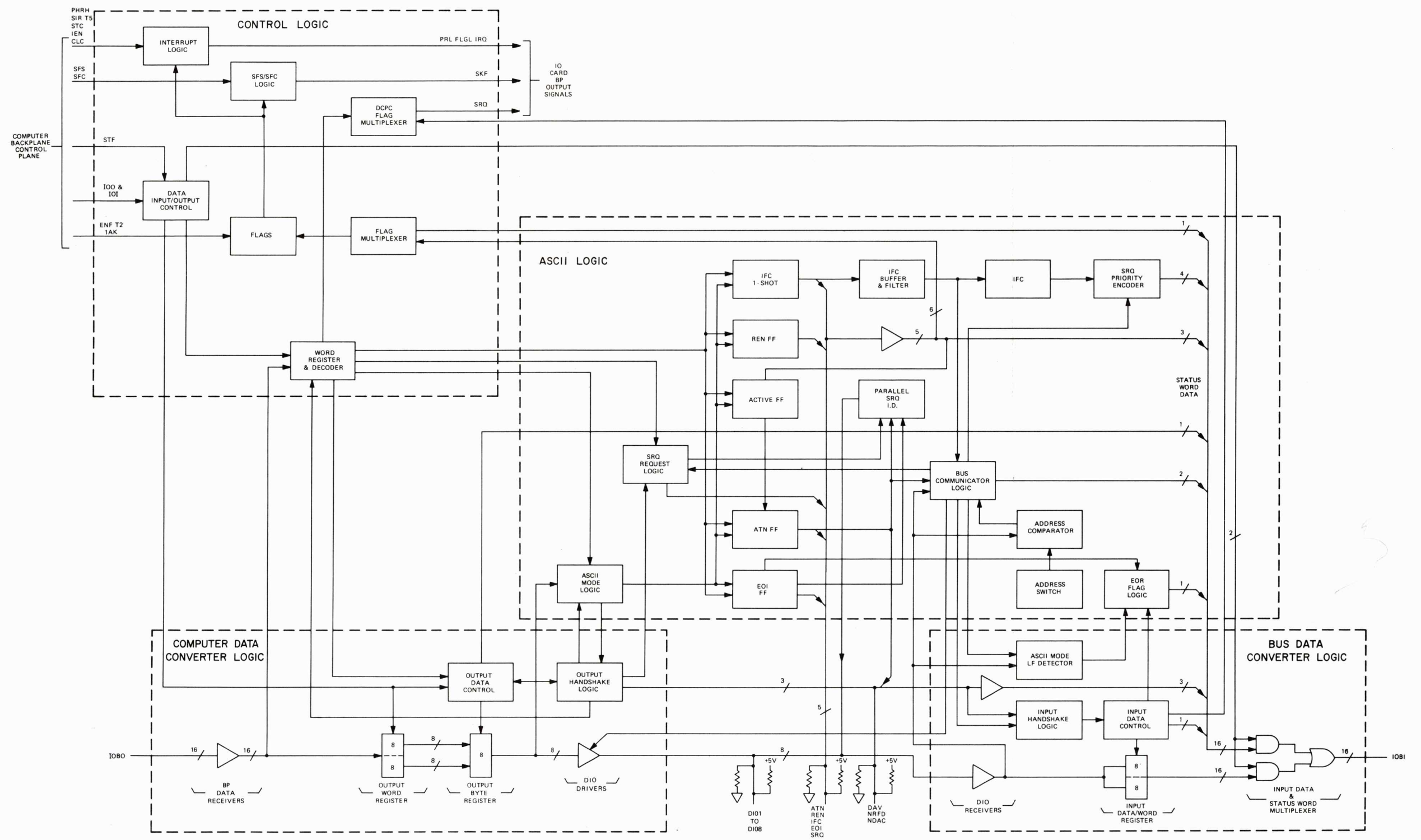
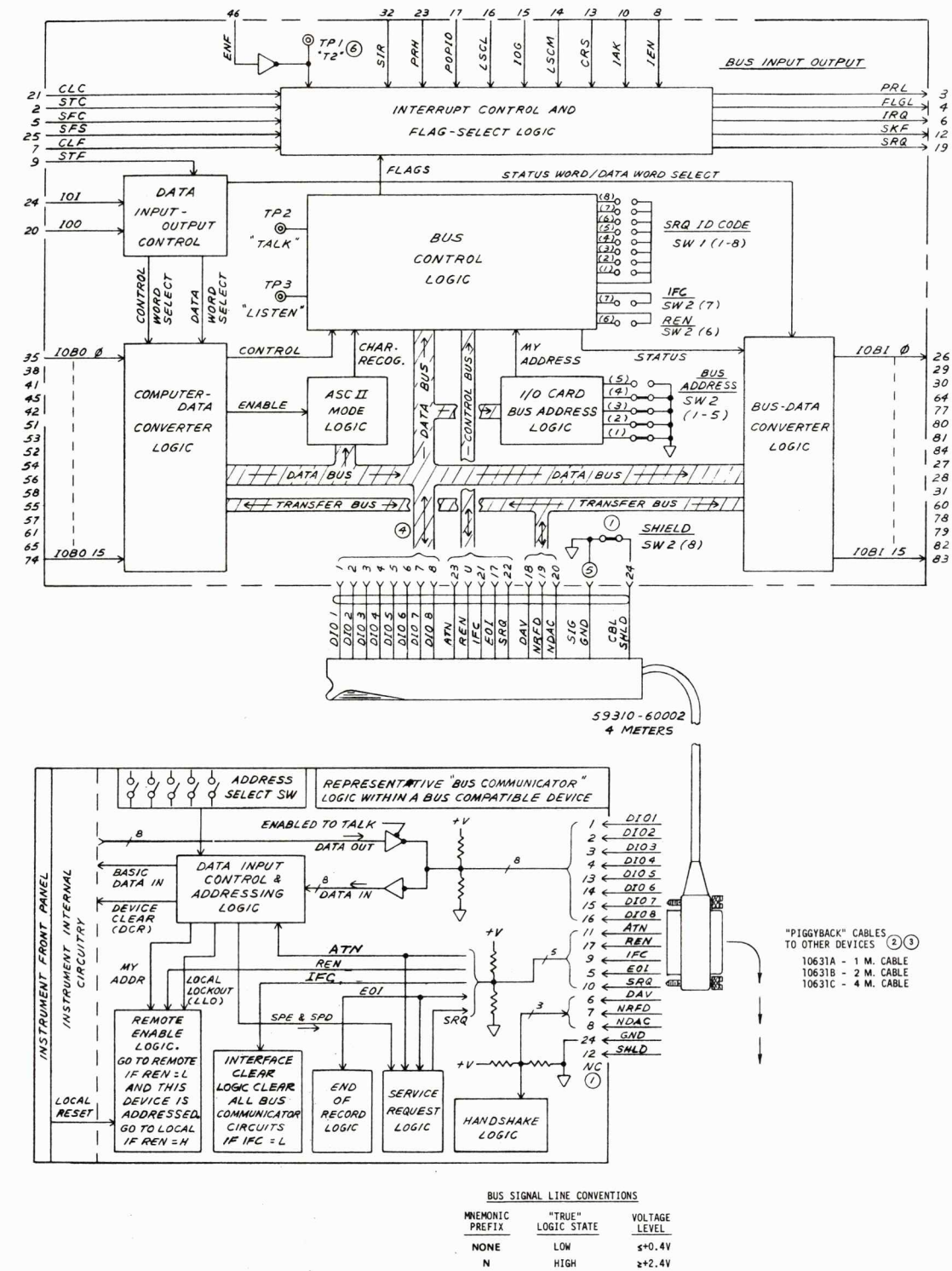


Figure 7-2. 59310B Interface Block Diagram



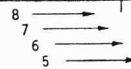
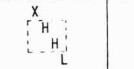
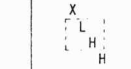

TEST-POINTS					
I/O CARD CONTROL WORD BIT #'s	CONTROL WORD FUNCTION	TEST-POINT TO VERIFY ACTION			
		ACCESS PT. ON CARD ⑥	CABLE PIN I/O	BUS	STATUS WD. BIT
2 - 8	IFC (100μs)	U41 (6) "I"	21	9	-
	REN	U43 (6) "I"	U	17	8
	ACTIVE	U21 (9) "I"	-	-	4
	FORCE INPUT CYCLE	U54 (7) "I"	-	-	-
	CLEAR I/O CARD	U54 (9) "I"	-	-	-
6 - 3	ATN	U21 (5) "I"	23	11	7
	EOL	U22 (6) "I"	17(7)	5(7)	-
	TALK	TP-2	-	-	5
	LISTEN	TP-3	-	-	6
11 - 8 (BIT 7 ENABLES)	ASCII MODE	U65 (10) "I"	22(7)	10(7)	-
	SRQ ENABLE	U65 (15) "I"	-	-	-
	DMA R/W SELECT	U65 (2) "I"	-	-	-
	PACKING/ UNPACKING	U65 (7) "I"	-	-	-
15 - 12 (BIT 7 ENABLES)	EOR FLAG EN.	U76 (15) "I"	-	-	12
	ORA FLAG EN.	U76 (10) "I"	-	-	13
	IRL FLAG EN.	U76 (7) "I"	-	-	14
	SEP FLAG EN.	U76 (2) "I"	-	-	15

- NOTES:
- ① The cable shield is grounded only once, and is done at the System Controller.
 - ② The maximum accumulated cable length (per bus) is 20 meters, total.
 - ③ A bus cable network must not exceed an average of one "standard load" device for each 2 meters of bus cable; i.e.:
TOTAL CABLE LENGTH < 2 meters/device
NUMBER OF DEVICES
Remember that the I/O card must be counted as one of the devices.
 - ④ The I/O card's circuitry has one "Standard Load" on each bus signal line.
 - ⑤ Bus cable signal grounds are connected to I/O card common at connector pins V,W,X,Y,Z,AA and BB.
 - ⑥ Use TP-1 (2100 time "t2") to sync 'scope for dynamic tests.
 - ⑦ State of these signal lines is dependent on other I/O card functions that are programmed.

Figure 7-3. 59310B Simplified Logic Diagram
(Sheet 1 of 2)

I/O CARD ASCII-MODE FUNCTIONS			
FUNCTION	CODE		
	ASCII (TTY KEY)	OCTAL	DECIMAL
IFC (100μs)	ESC (ESC) (B)	33	27.
REN = L	STX (CTRL-B)	2	2.
= H	ETX (CTRL-C)	3	3.
ATN = L	SQ (CTRL-N)	16	14.
= H	SI (CTRL-O)	17	15.

GENERAL BUS-CODE ALLOCATIONS WITHIN THE ASCII-CODE SET

DIO LINES				UNIVERSAL BUS COMMANDS			DEVICE LISTEN ADDRESS			DEVICE TALK ADDRESS											
																					
COLUMN → 0				1			2			3			4			5					
ROW ↓				OCTAL DECIMAL BUS COMMAND			OCTAL DECIMAL BUS COMMAND			OCTAL DECIMAL SYMBOLIC ADDRESS			OCTAL DECIMAL SYMBOLIC ADDRESS			OCTAL DECIMAL SYMBOLIC ADDRESS					
H	H	H	H	0	0	0.	20	16.	40	32.	SP	60	48.	0	100	64.	@	120	80.	P	
H	H	H	L	1	1	1.	21	17.	41	33.	:	61	49.	1	101	65.	A	121	81.	Q	
H	H	L	H	2	2	2.	22	18.	R*	42	34.	"	62	50.	2	102	66.	B	122	82.	R
H	H	L	L	3	3	3.	23	19.	R*	43	35.	#	63	51.	3	103	67.	C	123	83.	S
H	L	H	H	4	4	4.	24	20.	DCR	44	36.	\$	64	52.	4	104	68.	D	124	84.	T
H	L	H	L	5	5	5.	25	21.	45	37.	%	65	53.	5	105	69.	E	125	85.	U	
H	L	L	H	6	6	6.	26	22.	46	38.	&	66	54.	6	106	70.	F	126	86.	V	
H	L	L	L	7	7	7.	27	23.	47	39.	'	67	55.	7	107	71.	G	127	87.	G	
L	H	H	H	8	10	8.	30	24.	SPE	50	40.	(70	56.	8	110	72.	H	130	88.	X
L	H	H	L	9	11	9.	31	25.	SPD	51	41.)	71	57.	9	111	73.	I	131	89.	Y
L	H	L	H	10	12	10.	32	26.	52	42.	*	72	58.	:	112	74.	J	132	90.	Z	
L	H	L	L	11	13	11.	33	27.	53	43.	+	73	59.	;	113	75.	K	133	91.	[
L	L	H	H	12	14	12.	34	28.	R*	54	44.	,	74	60.	<	114	76.	L	134	92.	\
L	L	H	L	13	15	13.	35	29.	R*	55	45.	-	75	61.	=	115	77.	M	135	93.]
L	L	L	H	14	16	14.	36	30.	56	46.	.	76	62.	>	116	78.	N	136	94.	^	
L	L	L	L	15	17	15.	37	31.	57	47.	/	77	63.	?	117	79.	O	137	95.	_	
										UNLISTEN COMMAND						UNTALK COMMAND					
<div>H = High State. L = Low State. X = Unused when MRE is low.</div> <div>LL0 = Local Lockout. DCR = Device Clear. R* = Reserved for future assignment</div> <div>SPE = Status Poll Enable. SPD = Status Poll Disable. DIO = Data Input Output Signal Lines. DIO1-8</div> <div>NOTE THAT ASCII COLUMNS 6 AND 7 ARE NOT USED.</div>																					

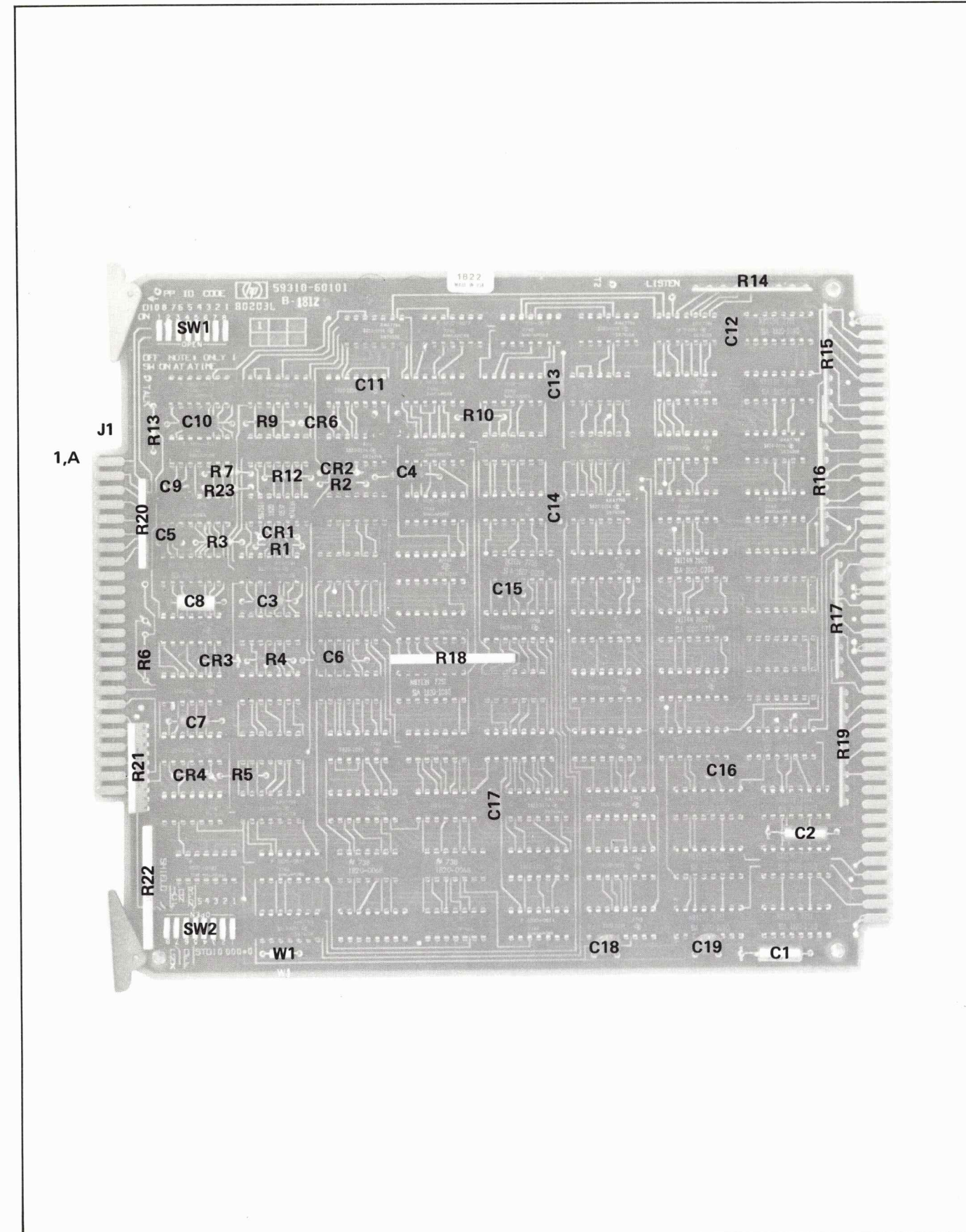
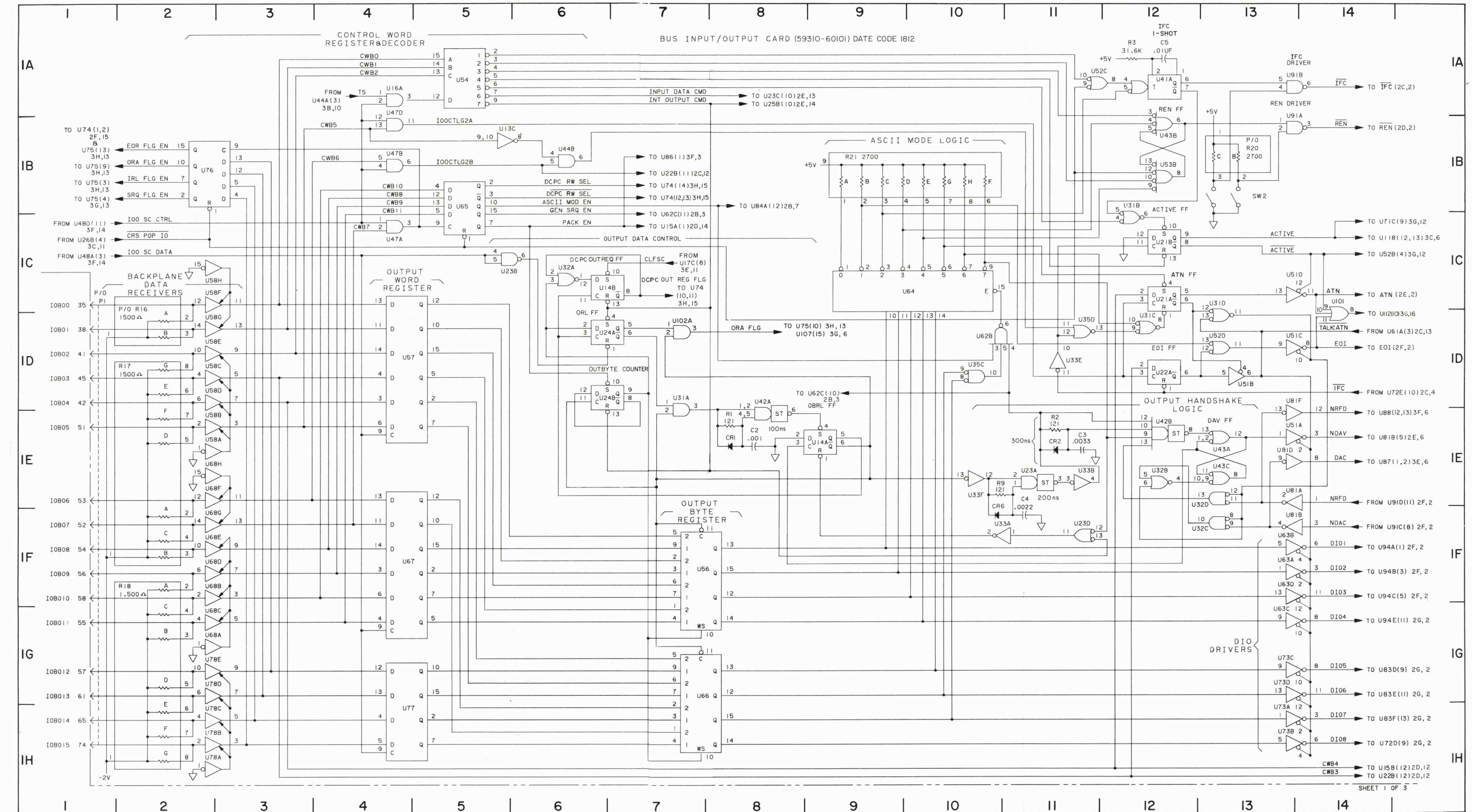
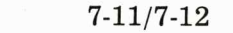


Figure 7-4. 59310B Component Locator

Figure 7-5. 59310B Schematic Diagram
(Sheet 1 of 3)



7-11/7-12



7-13/7-14

SALES & SERVICE OFFICES

AFRICA, ASIA, AUSTRALIA

ANGOLA

Teletra
Empresa Técnica de
Equipamentos
Eléctricos, S.A.R.L.
R. Barbosa Rodrigues, 42-1 DT.
Caixa Postal, 6487
Luanda
Tel: 35515/6
Cable: TELETRIA Luanda

AUSTRALIA

Hewlett-Packard Australia
Pty. Ltd.
31-41 Joseph Street
Blackburn, Victoria 3130
P.O. Box 36
Doncaster East, Victoria 3109
Tel: 89-6351
Telex: 31-024
Cable: HEWPAUD Melbourne

Pymble

Hewlett-Packard Australia
Pty. Ltd.
31 Bridge Street
Pymble
New South Wales, 2073
Tel: 449-8566
Telex: 21561
Cable: HEWPAUD Sydney

Hewlett-Packard Australia

Pty. Ltd.
153 Greenhill Road
Parkside, S.A. 5063
Tel: 272-5911
Telex: 82536 ADEL
Cable: HEWPAUD ADELAID
Hewlett-Packard Australia
Pty. Ltd.

141 Stirling Highway

Nedlands, W.A. 6009
Tel: 86-5455
Telex: 93859 PERTH
Cable: HEWPAUD PERTH
Hewlett-Packard Australia
Pty. Ltd.

121 Wollongong Street

Fyshwick, A.C.T. 2609
Tel: 95-2733
Telex: 62650 Canberra
Cable: HEWPAUD CANBERRA
Hewlett-Packard Australia
Pty. Ltd.

5th Floor

Teachers Union Building
495-499 Boundary Street
Spring Hill, 4000 Queensland
Tel: 229-1544
Cable: HEWPAUD Brisbane
GUAM
Medical/Pocket Calculators Only
Guam Medical Supply, Inc.
Jay Eise Building, Room 210
P.O. Box 8947
Tamuning 96911
Tel: 846-4513
Cable: EARMED Guam

HONG KONG

Schmidt & Co (Hong Kong) Ltd.
P.O. Box 297
Connaught Centre
39th Floor
Connaught Road, Central
Hong Kong
Tel: H-255291-5
Telex: 74766 SCHMC HX
Cable: SCHMIDTCO Hong Kong

INDIA

Blue Star Ltd.
Kasturji Buildings
Jamshedji Tata Rd
Bombay 400 020
Tel: 29 50 21
Telex: 001-2156
Cable: BLUEFROST

Blue Star Ltd.

Sahas
414/2 Vir Savarkar Marg
Prabhadevi
Bombay 400 025
Tel: 45 78 87
Telex: 011-4093
Cable: FROSTBLUE

Blue Star Ltd.

Band Box House
Prabhadevi
Bombay 400 025
Tel: 45 73 01
Telex: 011-3751
Cable: BLUESTAR

Blue Star Ltd.

7 Hare Street
P.O. Box 506
Calcutta 700 001
Tel: 23-0131
Telex: 021-7655
Cable: BLUESTAR

Blue Star Ltd.

7th & 8th Floor
Bhandari House
91 Nehru Place
New Delhi 110024
Tel: 634770 & 635166
Telex: 031-2463
Cable: BLUESTAR

Blue Star Ltd.

Meeakshi Mandir
xxx/1678 Mahatma Gandhi Rd.
Cochin 682 016
Tel: 32069, 32161, 32282
Telex: 0885-514
Cable: BLUESTAR

Blue Star Ltd.

1-1171
Sarajini Devi Road
Secunderabad 500 003
Tel: 70126, 70127
Cable: BLUEFROST
Telex: 0462-24-052

Blue Star Ltd.

2/34 Kodambakkam High Road
Madras 600034
Tel: 82056
Telex: 041-379
Cable: BLUESTAR

INDONESIA

BERCA Indonesia P.T.
P.O. Box 496/JKT
Jl. Na'Abdul Muhsin 62
Jakarta
Tel: 40369, 49886, 49255, 356038
JKT 42895
Cable: BERCACON
BERCA Indonesia P.T.
63 J.L. Raya Gubeng
Surabaya
Tel: 44309

ISRAEL

Electronics & Engineering Div.
of Motorola Israel Ltd.
17, Kremetstki Street
P.O. Box 25016
Tel-Aviv
Tel: 35569
Cable: BASTEL Tel-Aviv

JAPAN

Yokogawa-Hewlett-Packard Ltd.
Ohashi Building
59-1 Yoyogi 1-Chome
Shibuya-ku, Tokyo 151
Tel: 03-370-2281/92
Telex: 232-2024YHP MARKET
TOK 73-724
Cable: YHPMARKET

Yokogawa-Hewlett-Packard Ltd.

Chuo Bldg., 4th Floor
4-20 Nishinakajima 5-chome
Yodogawa-ku, Osaka-shi
Osaka 532
Tel: 06-304-6021

Yokogawa-Hewlett-Packard Ltd.

Nakamo Building
24 Kami Sasajima-cho
Nakamura-ku, Nagoya 450
Tel: (052) 571-5171
Yokogawa-Hewlett-Packard Ltd.
Tangway Building
2-24-1 Tsuruya-cho
Kanagawa-ku
Yokohama 221
Tel: 045-312-1252
Telex: 382-3204 YHP YOK

Yokogawa-Hewlett-Packard Ltd.

Mito Mitsui Building
105, Chome-1, San-no-maru
Mito, Ibaragi 310
Tel: 0292-25-7470
Yokogawa-Hewlett-Packard Ltd.
Inoue Building
1348-3, Asahi-cho, 1-chome
Atsugi, Kanagawa 243
Tel: 0462-24-052

Yokogawa-Hewlett-Packard Ltd.

Kumagaya Asahi
Hackjuni Building
4th Floor
3-4, Tsukuba
Kumagaya, Saitama 360
Tel: 0485-24-6563

KENYA

Technical Engineering
Services (E.A.) Ltd.
P.O. Box 18311
Nairobi
Tel: 557726-556762
Cable: PROTION
Medical Only
International Aeradio (E.A.) Ltd.
P.O. Box 19012
Nairobi Airport
Nairobi
Tel: 336055/56
Telex: 22201/22301
Cable: INTAERIO Nairobi

KOREA

Samsung Electronics Co., Ltd.
20th Fl. Dongbang Bldg. 250, 2-KA
C.P.O. Box 2775
Taeyung-Ro, Chung-Ku
Seoul
Tel: (23) 6811
Telex: 22575
Cable: ELEKSTAR Seoul

MALESIA

Teknik Mutu Sdn. Bhd.
2 Lorong 13/6A
Section 13
Petaling Jaya, Selangor
Tel: 54994/54996
Telex: MA 37605
Protel Engineering
P.O. Box 197
Lot 259, Satok Road
Kuching, Sarawak
Tel: 2400
Cable: PROTENG

MOZAMBIQUE

A.N. Goncalves, Lda
162, 1 Apt. 14 Av. D. Luis
Caixa Postal 107
Lourenco Marques
Tel: 27091, 27114
Telex: 6-203 NEGON Mo
Cable: NEGON

NEW ZEALAND

Hewlett-Packard (N.Z.) Ltd.
P.O. Box 9443
Courtenay Place
Wellington
Tel: 877-199
Cable: HEWPAUD Wellington
Hewlett-Packard (N.Z.) Ltd.
Pakuranga Professional Centre
267 Pakuranga Highway
Box 51092
Pakuranga
Tel: 869-651
Cable: HEWPAUD Auckland

Analytical/Medical Only
Medical Supplies N.Z. Ltd.
Scientific Division
79 Carlton Gore Rd., Newmarket
P.O. Box 1234
Auckland
Tel: 75-289
Cable: DENTAL Auckland

Analytical/Medical Only
Medical Supplies N.Z. Ltd.
P.O. Box 1994
147-161 Tory St.
Wellington
Tel: 850-799
Telex: 3858
Cable: DENTAL, Wellington

Analytical/Medical Only
Medical Supplies N.Z. Ltd.
P.O. Box 309
239 Stanmore Road
Christchurch
Tel: 892-019
Cable: DENTAL, Christchurch

Analytical/Medical Only
Medical Supplies N.Z. Ltd.
P.O. Box 233
Dunedin
Tel: 88-817
Cable: DENTAL, Dunedin

NIGERIA
The Electronics
Instrumentations Ltd.
N6B-770 Oyo Road
Idumose House
P.M.B. 5402
Ibadan
Tel: 61577
Telex: 31231 TEIL Nigeria
Cable: THETEIL Ibadan

The Electronics Instrumenta-
tions Ltd.
144 Agege Motor Road, Mushin
P.O. Box 6645
Lagos
Cable: THETEIL Lagos

PAKISTAN
Mushko & Company, Ltd.
Oosheen Chambers
Abdullah Haroon Road
Karachi-3
Tel: 511027, 512927
Telex: 2694
Cable: COOPERATOR Karachi

Mushko & Company, Ltd.
38B, Satellite Town
Rawalpindi
Tel: 41924
Cable: FEMUS Rawalpindi

PHILIPPINES
The Online Advanced
Systems Corporation
Rico House
Amorsolo cor. Herrera Str.
Legaspi Village, Makati
Metro Manila
Tel: 85-35-81, 85-34-91
Telex: 3274 ONLINE

RHODESIA

Field Technical Sales
45 Kelvin Road North
P.O. Box 3458
Salisbury
Tel: 705231 (5 lines)
Telex: RH 4122

SINGAPORE

Hewlett-Packard Singapore
(Pte.) Ltd.
1150 Depot Road
Alexandra P.O. Box 58
Singapore 4
Tel: 270-2355
Telex: HPSG RS 21486
Cable: HEWPAUD, Singapore

SOUTH AFRICA

Hewlett-Packard South Africa
(Pty.) Ltd.
Private Bag Wendywood
Sandton, Transvaal 2144
Hewlett-Packard Centre
Daphne Street, Wendywood.
Sandton, Transvaal 2144
Tel: 802-10408
Telex: 8-4782
Cable: HEWPAUD JOHANNESBURG

Service Department
Hewlett-Packard South Africa
(Pty.) Ltd.
P.O. Box 39325
Gramley, Sandton, 2018
451 Wyndberg Extension 3.
Sandton, 2001
Tel: 636-8188/9
Telex: 8-2391

Hewlett-Packard South Africa
(Pty.) Ltd.
P.O. Box 120
Howard Place, Cape Province, 7450
Pine Park Centre, Forest Drive.
Pinelands, Cape Province, 7405
Tel: 53-7955 thu 9
Telex: 57-0006

Service Department
Hewlett-Packard South Africa
(Pty.) Ltd.
P.O. Box 37099
Overport, Durban 4067
Brady House
641 Ridge Road
Durban, 4001
Tel: 88-7478
Telex: 6-7954

TAIWAN
Hewlett-Packard Far East Ltd.,
Taiwan Branch
39 Chung Hsiao West Road
Sec. 1, 7th Floor
Taipei
Tel: 3819160-4
Cable: HEWPAUD TAIPEI

Hewlett-Packard Far East Ltd.
Taiwan Branch
68-2, Chung Cheng 3rd Road
Kaohsiung
Tel: (07) 242318-Kaohsiung

Analytical Only
San Kwang Instruments Co., Ltd.,
No. 20, Yung Sui Road
Taipei
Tel: 371571-4 (5 lines)
Telex: 22894 SANKWANG
Cable: SANKWANG TAIPEI

TANZANIA
Medical Only
International Aeradio (E.A.) Ltd.
P.O. Box 861
Dar es Salaam
Tel: 21251 Ext. 265
Telex: 41030

THAILAND
UNIMESA Co., Ltd.
Elcom Research Building
2538 Sukumvit Ave.
Bangkok
Tel: 393297, 3930338
Cable: UNIMESA Bangkok

UGANDA
Medical Only
International Aeradio (E.A.) Ltd.,
P.O. Box 2577
Kampala
Tel: 54388
Cable: INTAERIO Kampala

ZAMBIA
R.J. Tibury (Zambia) Ltd.
P.O. Box 2792
Lusaka
Tel: 73793
Cable: ARJAYTEE, Lusaka

OTHER AREAS NOT LISTED, CONTACT:

Hewlett-Packard Intercontinental
3200 Hillview Ave.
Palo Alto, California 94304
Tel: (415) 493-1501
TWX: 910-373-1267
Cable: HEWPAUD Palo Alto

FOR CANADIAN AREAS NOT LISTED:
Contact Hewlett-Packard (Canada)
Ltd. in Mississauga.

FOR AREAS NOT LISTED, CONTACT:
Hewlett-Packard
Inter-Americas
3200 Hillview Ave.
Palo Alto, California 94304
Tel: (415) 493-1501
TWX: 910-373-1267
Cable: HEWPAUD Palo Alto

FOR AREAS NOT LISTED, CONTACT:
Hewlett-Packard
Inter-Americas
3200 Hillview Ave.
Palo Alto, California 94304
Tel: (415) 493-1501
TWX: 910-373-1267
Cable: HEWPAUD Palo Alto

FOR AREAS NOT LISTED, CONTACT:
Hewlett-Packard
Inter-Americas
3200 Hillview Ave.
Palo Alto, California 94304
Tel: (415) 493-1501
TWX: 910-373-1267
Cable: HEWPAUD Palo Alto

FOR AREAS NOT LISTED, CONTACT:
Hewlett-Packard
Inter-Americas
3200 Hillview Ave.
Palo Alto, California 94304
Tel: (415) 493-1501
TWX: 910-373-1267
Cable: HEWPAUD Palo Alto

FOR AREAS NOT LISTED, CONTACT:
Hewlett-Packard
Inter-Americas
3200 Hillview Ave.
Palo Alto, California 94304
Tel: (415) 493-1501
TWX: 910-373-1267
Cable: HEWPAUD Palo Alto

FOR AREAS NOT LISTED, CONTACT:
Hewlett-Packard
Inter-Americas
3200 Hillview Ave.
Palo Alto, California 94304
Tel: (415) 493-1501
TWX: 910-373-1267
Cable: HEWPAUD Palo Alto

FOR AREAS NOT LISTED, CONTACT:
Hewlett-Packard
Inter-Americas
3200 Hillview Ave.
Palo Alto, California 94304
Tel: (415) 493-1501
TWX: 910-373-1267
Cable: HEWPAUD Palo Alto

FOR AREAS NOT LISTED, CONTACT:
Hewlett-Packard
Inter-Americas
3200 Hillview Ave.
Palo Alto, California 94304
Tel: (415) 493-1501
TWX: 910-373-1267
Cable: HEWPAUD Palo Alto

FOR AREAS NOT LISTED, CONTACT:
Hewlett-Packard
Inter-Americas
3200 Hillview Ave.
Palo Alto, California 94304
Tel: (415) 493-1501
TWX: 910-373-1267
Cable: HEWPAUD Palo Alto

FOR AREAS NOT LISTED, CONTACT:
Hewlett-Packard
Inter-Americas
3200 Hillview Ave.
Palo Alto, California 94304
Tel: (415) 493-1501
TWX: 910-373-1267
Cable: HEWPAUD Palo Alto

FOR AREAS NOT LISTED, CONTACT:
Hewlett-Packard
Inter-Americas
3200 Hillview Ave.
Palo Alto, California 94304
Tel: (415) 493-1501
TWX: 910-373-1267
Cable: HEWPAUD Palo Alto

FOR AREAS NOT LISTED, CONTACT:
Hewlett-Packard
Inter-Americas
3200 Hillview Ave.
Palo Alto, California 94304
Tel: (415) 493-1501
TWX: 910-373-1267
Cable: HEWPAUD Palo Alto

FOR AREAS NOT LISTED, CONTACT:
Hewlett-Packard
Inter-Americas
3200 Hillview Ave.
Palo Alto, California 94304
Tel: (415) 493-1501
TWX: 910-373-1267
Cable: HEWPAUD Palo Alto

FOR AREAS NOT LISTED, CONTACT:
Hewlett-Packard
Inter-Americas
3200 Hillview Ave.
Palo Alto, California 94304
Tel: (415) 493-1501
TWX: 910-373-1267
Cable: HEWPAUD Palo Alto

FOR AREAS NOT LISTED, CONTACT:
Hewlett-Packard
Inter-Americas
3200 Hillview Ave.
Palo Alto, California 94304
Tel: (415) 493-1501
TWX: 910-373-1267
Cable: HEWPAUD Palo Alto

FOR AREAS NOT LISTED, CONTACT:
Hewlett-Packard
Inter-Americas
3200 Hillview Ave.
Palo Alto, California 94304
Tel: (415) 493-1501
TWX: 910-373-1267
Cable: HEWPAUD Palo Alto

FOR AREAS NOT LISTED, CONTACT:
Hewlett-Packard
Inter-Americas
3200 Hillview Ave.
Palo Alto, California 94304
Tel: (415) 493-1501
TWX: 910-373-1267
Cable: HEWPAUD Palo Alto

FOR AREAS NOT LISTED, CONTACT:
Hewlett-Packard
Inter-Americas
3200 Hillview Ave.
Palo Alto, California 94304
Tel: (415) 493-1501
TWX: 910-373-1267
Cable: HEWPAUD Palo Alto

FOR AREAS NOT LISTED, CONTACT:
Hewlett-Packard
Inter-Americas
3200 Hillview Ave.
Palo Alto, California 94304
Tel: (415) 493-1501
TWX: 910-373-1267
Cable: HEWPAUD Palo Alto

FOR AREAS NOT LISTED, CONTACT:
Hewlett-Packard
Inter-Americas
3200 Hillview Ave.
Palo Alto, California 94304
Tel: (415) 493-1501
TWX: 910-373-1267
Cable: HEWPAUD Palo Alto

FOR AREAS NOT LISTED, CONTACT:
Hewlett-Packard
Inter-Americas
3200 Hillview Ave.
Palo Alto, California 94304
Tel: (415) 493-1501
TWX: 910-373-1267
Cable: HEWPAUD Palo Alto

FOR AREAS NOT LISTED, CONTACT:
Hewlett-Packard
Inter-Americas
3200 Hillview Ave.
Palo Alto, California 94304
Tel: (415) 493-1501
TWX: 910-373-1267
Cable: HEWPAUD Palo Alto

FOR AREAS NOT LISTED, CONTACT:
Hewlett-Packard
Inter-Americas
3200 Hillview Ave.
Palo Alto, California 94304
Tel: (415) 493-1501
TWX: 910-373-1267
Cable: HEWPAUD Palo Alto

FOR AREAS NOT LISTED, CONTACT:
Hewlett-Packard
Inter-Americas
3200 Hillview Ave.
Palo Alto, California 94304
Tel: (415) 493-1501
TWX: 910-373-1267
Cable: HEWPAUD Palo Alto

FOR AREAS NOT LISTED, CONTACT:
Hewlett-Packard
Inter-Americas
3200 Hillview Ave.
Palo Alto, California 94304
Tel: (415) 493-1501
TWX: 910-373-1267
Cable: HEWPAUD Palo Alto

FOR AREAS NOT LISTED, CONTACT:
Hewlett-Packard
Inter-Americas
3200 Hillview Ave.
Palo Alto, California 94304
Tel: (415) 493-1501
TWX: 910-373-1267
Cable: HEWPAUD Palo Alto

FOR AREAS NOT LISTED, CONTACT:
Hewlett-Packard
Inter-Americas
3200 Hillview Ave.
Palo Alto, California 94304
Tel: (415) 493-1501
TWX: 910-373-1267
Cable: HEWPAUD Palo Alto

FOR AREAS NOT LISTED, CONTACT:
Hewlett-Packard
Inter-Americas
3200 Hillview Ave.
Palo Alto, California 94304
Tel: (415) 493-1501
TWX: 910-373-1267
Cable: HEWPAUD Palo Alto

FOR AREAS NOT LISTED, CONTACT:
Hewlett-Packard
Inter-Americas
3200 Hillview Ave.
Palo Alto, California 94304
Tel: (415) 493-1501
TWX: 910-373-1267
Cable: HEWPAUD Palo Alto

FOR AREAS NOT LISTED, CONTACT:
Hewlett-Packard
Inter-Americas
3200 Hillview Ave.
Palo Alto, California 94304
Tel: (415) 493-1501
TWX: 910-373-1267
Cable: HEWPAUD Palo Alto

FOR AREAS NOT LISTED, CONTACT:
Hewlett-Packard
Inter-Americas
3200 Hillview Ave.
Palo Alto, California 94304
Tel: (415) 493-1501
TWX: 910-373-1267
Cable: HEWPAUD Palo Alto

FOR AREAS NOT LISTED, CONTACT:
Hewlett-Packard
Inter-Americas
3200 Hillview Ave.
Palo Alto, California 94304
Tel: (415) 493-1501
TWX: 910-373-1267
Cable: HEWPAUD Palo Alto

FOR AREAS NOT LISTED, CONTACT:
Hewlett-Packard
Inter-Americas
3200 Hillview Ave.
Palo Alto, California 94304
Tel: (415) 493-1501
TWX: 910-373-1267
Cable: HEWPAUD Palo Alto

FOR AREAS NOT LISTED, CONTACT:
Hewlett-Packard
Inter-Americas
3200 Hillview Ave.
Palo Alto, California 94304
Tel: (415) 493-1501
TWX: 910-373-1267
Cable: HEWPAUD Palo Alto

FOR AREAS NOT LISTED, CONTACT:
Hewlett-Packard
Inter-Americas
3200 Hillview Ave.
Palo Alto, California 94304
Tel: (415) 493-1501
TWX: 910-373-1267
Cable: HEWPAUD Palo Alto

FOR AREAS NOT LISTED, CONTACT:
Hewlett-Packard
Inter-Americas
3200 Hillview Ave.
Palo Alto, California 94304
Tel: (415) 493-1501
TWX: 910-373-1267
Cable: HEWPAUD Palo Alto

FOR AREAS NOT LISTED, CONTACT:
Hewlett-Packard
Inter-Americas
3200 Hillview Ave.
Palo Alto, California 94304
Tel: (415) 493-1501
TWX: 910-373-1267
Cable: HEWPAUD Palo Alto

FOR AREAS NOT LISTED, CONTACT:
Hewlett-Packard
Inter-Americas
3200 Hillview Ave.
Palo Alto, California 94304
Tel: (415) 493-1501
TWX: 910-373-1267
Cable: HEWPAUD Palo Alto

CANADA

EUROPE, NORTH AFRICA AND MIDDLE EAST

AUSTRIA

Hewlett-Packard Ges.m.b.H.
Handelskai 52
P.O. Box 7
A-1205 Vienna
Tel. (0222) 351621 to 27
cable: HEWPAK Vienna
Telex: 75923 hewpak a

BELGIUM

Hewlett-Packard Benelux
S.A. N.V.
Avenue de Col-Vert, 1.
(Groenkruglaan)
B-1170 Brussels
Tel. (02) 672 22 40
Cable: PALOBEN Brussels
Telex: 23 494 paloben bru

CYPRUS

Nykionics
19 Gregorios & Xenopoulos Rd.
P.O. Box 1152
Cy-Nicosia
Tel. 45628/29
Cable: KYPRONICS PANDEHS
Telex: 3018

CZECHOSLOVAKIA

Vývojová a Provozni Základna
Výzkumných Ústavů v Bechovicích
CSSR-25097 Bechovice u Prahy
Tel. 89 93 41
Telex: 121333
Institute of Medical Bionics
Výzkumný Ústav Lékařské Bioniky
Jedlova 6
CS-88346 Bratislava-Kramare
Tel. 44-551/45-541

DDR

Entwicklungslabor der TU Dresden
Forschungsinstitut Meinsberg
DDR-7305
Waldheim/Meinsberg
Tel. 37 667
Telex: 112145

Export Contact AG Zuerich
Guenther Forger
Schlegelstrasse 15
1040 Berlin
Tel. 42-74-12
Telex: 111889

DENMARK

Hewlett-Packard A/S
Datavej 52
DK-3460 Birkerød
Tel. (02) 81 66 40
Cable: HEWPAK AS
Telex: 37409 hpas dk
Hewlett-Packard A/S
Navevej 1
DK-8600 Silkeborg
Tel. (06) 82 71 66
Telex: 37409 hpas dk
Cable: HEWPAK AS

FINLAND

Hewlett-Packard OY
Nankkousuntie 5
P.O. Box 5
SF-00211 Helsinki 21
Tel. (90) 6923031
Cable: HEWPAK OY Helsinki
Telex: 12-1563 HEWPA SF

FRANCE

Hewlett-Packard France
Quartier de Courtaubert
Boite Postale No. 6
F-91041 Orsay Cedex
Tel. (1) 90 78 25
Cable: HEWPAK Orsay
Telex: 600048
Hewlett-Packard France
Agence Régionale
"Le Saquin"
Chemin des Mouilles
B.P. 162
F-69130 Ecully
Tel. (78) 33 81 25
Cable: HEWPAK Ecully
Telex: 31 06 17

Hewlett-Packard France
Agence Régionale
Périmètre de la Cédre
Chemin de la Cédre, 20
F-31300 Toulouse-Le Mirail
Tel. (61) 40 11 12
Cable: HEWPAK 51957
Telex: 510957

Hewlett-Packard France
Agence Régionale
Aéroport principal de
Marseille-Marganne
F-13721 Marignane
Tel. (91) 89 12 36
Cable: HEWPAK MARGN
Telex: 410770
Hewlett-Packard France
Agence Régionale
63, Avenue de Rochester
B.P. 1124
F-35014 Rennes Cedex
Tel. (99) 36 33 21
Cable: HEWPAK 74912
Telex: 740912

Hewlett-Packard France
Agence Régionale
74, Allée de la Robertsau
F-67000 Strasbourg
Tel. (88) 35 23 20/21
Cable: HEWPAK STRBG
Telex: 121333

Hewlett-Packard France
Agence Régionale
Centre Vauban
201, rue Colbert
F-67000 Strasbourg
Tel. (88) 35 23 20/21
Cable: HEWPAK STRBG
Telex: 121333

Hewlett-Packard France
Agence Régionale
Centre Vauban
201, rue Colbert
F-67000 Strasbourg
Tel. (88) 35 23 20/21
Cable: HEWPAK STRBG
Telex: 121333

Hewlett-Packard France
Agence Régionale
Centre Vauban
201, rue Colbert
F-67000 Strasbourg
Tel. (88) 35 23 20/21
Cable: HEWPAK STRBG
Telex: 121333

Hewlett-Packard France
Agence Régionale
Centre Vauban
201, rue Colbert
F-67000 Strasbourg
Tel. (88) 35 23 20/21
Cable: HEWPAK STRBG
Telex: 121333

Hewlett-Packard France
Agence Régionale
Centre Vauban
201, rue Colbert
F-67000 Strasbourg
Tel. (88) 35 23 20/21
Cable: HEWPAK STRBG
Telex: 121333

Hewlett-Packard France
Agence Régionale
Centre Vauban
201, rue Colbert
F-67000 Strasbourg
Tel. (88) 35 23 20/21
Cable: HEWPAK STRBG
Telex: 121333

Hewlett-Packard France
Agence Régionale
Centre Vauban
201, rue Colbert
F-67000 Strasbourg
Tel. (88) 35 23 20/21
Cable: HEWPAK STRBG
Telex: 121333

Hewlett-Packard France
Agence Régionale
Centre Vauban
201, rue Colbert
F-67000 Strasbourg
Tel. (88) 35 23 20/21
Cable: HEWPAK STRBG
Telex: 121333

Hewlett-Packard GmbH
Werk Grotzingen
Ohmstrasse 6
D-7500 Karlsruhe 41
Tel. (0721) 69 40 06
Telex: 07-825707

Hewlett-Packard GmbH
Technisches Büro Nürnberg
Neumeyer Str. 90
D-8500 Nürnberg
Tel. (0911) 56 30 83/85
Telex: 0623 860
Hewlett-Packard GmbH
Technisches Büro München
Unterfächinger Strasse 28
ISAR Center
D-8012 Ottobrunn
Tel. (089) 601 30 61/7
Cable: HEWPAKSA München
Telex: 0524985

Hewlett-Packard GmbH
Technisches Büro Berlin
Keith Strasse 2-4
D-1000 Berlin 30
Tel. (030) 24 90 86
Telex: 18 3405 hpbm d

GREECE

Kostas Karayannis
GR - Omirou Street
GR - Athens 133
Tel. 3237731
Cable: RAKAR Athens
Tel. 21 59 62 rka gr
Analytical Only
"INTECO" G. Papathanassiou & Co.
Marin 17
GR - Athens 103
Tel. 252 1915
Cable: INTERNIKA Athens
Telex: 21 5329 INTE GR

Hewlett-Packard GmbH
Technisches Büro Berlin
Keith Strasse 2-4
D-1000 Berlin 30
Tel. (030) 24 90 86
Telex: 18 3405 hpbm d

Hewlett-Packard GmbH
Technisches Büro München
Unterfächinger Strasse 28
ISAR Center
D-8012 Ottobrunn
Tel. (089) 601 30 61/7
Cable: HEWPAKSA München
Telex: 0524985

Hewlett-Packard GmbH
Technisches Büro Nürnberg
Neumeyer Str. 90
D-8500 Nürnberg
Tel. (0911) 56 30 83/85
Telex: 0623 860

Hewlett-Packard GmbH
Technisches Büro München
Unterfächinger Strasse 28
ISAR Center
D-8012 Ottobrunn
Tel. (089) 601 30 61/7
Cable: HEWPAKSA München
Telex: 0524985

Hewlett-Packard GmbH
Technisches Büro Nürnberg
Neumeyer Str. 90
D-8500 Nürnberg
Tel. (0911) 56 30 83/85
Telex: 0623 860

Hewlett-Packard GmbH
Technisches Büro München
Unterfächinger Strasse 28
ISAR Center
D-8012 Ottobrunn
Tel. (089) 601 30 61/7
Cable: HEWPAKSA München
Telex: 0524985

ITALY

Hewlett-Packard Italiana S.p.A.
Via Amerigo Vesputci 2
Casella postale 3645
I-20100 Milano
Tel. (2) 6251 (10 lines)
Cable: HEWPAKIT Milano
Telex: 32046

Hewlett-Packard Italiana S.p.A.
Via Pietro Maroncelli 40
(ang. Via Visentin)
I-35100 Padova
Tel. (49) 86 48 88
Telex: 41612 Hewpacki
Medical only
Hewlett-Packard Italiana S.p.A.
Via d'Aghardi, 7
I-56100 Pisa
Tel. (050) 2 32 04
Telex: 32046 Via Milano

Hewlett-Packard Italiana S.p.A.
Via G. Arminelli 10
I-00143 Roma
Tel. (06) 54 69 61
Telex: 61514
Cable: HEWPAKIT Roma
Hewlett-Packard Italiana S.p.A.
Corso Giovanni Lanza
I-1031 Torino
Tel. (011) 682245/659308

Medical/Calculators Only
Hewlett-Packard Italiana S.p.A.
Via Principe Nicola 43 G/C
I-95126 Catania
Tel. (095) 37 05 04
Hewlett-Packard Italiana S.p.A.
Via Amerigo Vesputci, 9
I-80142 Napoli
Tel. (081) 33 77 11

Hewlett-Packard Italiana S.p.A.
Via E. Masi, 9/8
I-40137 Bologna
Tel. (051) 30 76 87
Hewlett-Packard Italiana S.p.A.
Via Amerigo Vesputci, 9
I-80142 Napoli
Tel. (081) 33 77 11

Hewlett-Packard Italiana S.p.A.
Via E. Masi, 9/8
I-40137 Bologna
Tel. (051) 30 76 87
Hewlett-Packard Italiana S.p.A.
Via Amerigo Vesputci, 9
I-80142 Napoli
Tel. (081) 33 77 11

Hewlett-Packard Italiana S.p.A.
Via E. Masi, 9/8
I-40137 Bologna
Tel. (051) 30 76 87
Hewlett-Packard Italiana S.p.A.
Via Amerigo Vesputci, 9
I-80142 Napoli
Tel. (081) 33 77 11

Hewlett-Packard Italiana S.p.A.
Via E. Masi, 9/8
I-40137 Bologna
Tel. (051) 30 76 87
Hewlett-Packard Italiana S.p.A.
Via Amerigo Vesputci, 9
I-80142 Napoli
Tel. (081) 33 77 11

Hewlett-Packard Italiana S.p.A.
Via E. Masi, 9/8
I-40137 Bologna
Tel. (051) 30 76 87
Hewlett-Packard Italiana S.p.A.
Via Amerigo Vesputci, 9
I-80142 Napoli
Tel. (081) 33 77 11

Hewlett-Packard Italiana S.p.A.
Via E. Masi, 9/8
I-40137 Bologna
Tel. (051) 30 76 87
Hewlett-Packard Italiana S.p.A.
Via Amerigo Vesputci, 9
I-80142 Napoli
Tel. (081) 33 77 11

Hewlett-Packard Italiana S.p.A.
Via E. Masi, 9/8
I-40137 Bologna
Tel. (051) 30 76 87
Hewlett-Packard Italiana S.p.A.
Via Amerigo Vesputci, 9
I-80142 Napoli
Tel. (081) 33 77 11

POLAND

Burow Informatyki Technicznej
Hewlett-Packard
Ul. Stawki 2, 6P
00-950 Warszawa
Tel. 395962/395187
Telex: 81 24 53 hcpa pl

UNIPAN

Zakład nadzoru i kontroli
Budowy Aparatury Naukowej
Ul. Krajowej Rady Narodowej 51/55
00-800 Warszawa
Tel. 36190
Telex: 81 46 48
Zakłady Naprawcze Sprzetu
Medycznego
Plac Komuny Paryskiej 6
90-007 Lodz
Tel. 334-41, 337-83

PORTUGAL

Teletra-Empresa Técnica de
Equipamentos Electronicos S. a. l.
Rua Rodrigo da Fonseca 103
P.O. Box 2531
P. Lisbon
Tel. (1) 68 60 72
Cable: TELETRA Lisbon
Telex: 12598

Medical only
Mundinter
Intercambio Mundial de Comercio
S. a. l.
Av. A. de Aguiar 138
P.O. Box 2761
P. Lisbon
Tel. (19) 53 21 31/7
Cable: INTERCAMBIO Lisbon

ROMANIA

Hewlett-Packard Reprezentanta
Bd. N. Balcescu 16
Bucharest
Tel. (01) 58023/138885
Telex: 10440

TURKEY

Telekom Engineering Bureau
P.O. Box 437
Beyoglu
P.O. Box 101000
Moscow
Tel. 49 40 40
Cable: TELEMATON Istanbul
Telex: 23609

SAUDI ARABIA

Modern Electronic Establishment
King Abdul Aziz str. (Head office)
P.O. Box 1228
Jeddah
Tel. 31173-332201
Cable: ELECTRA
P.O. Box 2728 (Service center)
Riyadh
Tel. 62596-66232
Cable: RAOUFCO

SPAIN

Hewlett-Packard Española, S.A.
Jerre, Calle 3
E-Madrid 16
Tel. (1) 458 26 00 (10 lines)
Telex: 23515 hpe
Hewlett-Packard Española, S.A.
Mianesado 21-23
E-Barcelona 17
Tel. (3) 203 6200 (5 lines)
Telex: 52603 hpe e

MOROCCO

Gerep
190, Blvd. Ibrahim Roudani
Casablanca
Tel. 25-16-76/25-90-99
Cable: Gerep-Casa
Telex: 23739

NETHERLANDS

Hewlett-Packard Benelux N.V.
Van Heuven Goedhartlaan 121
P.O. Box 561
NL-1134 Amstelveen
Tel. (020) 47 20 21
Cable: PALOBEN Amsterdam
Telex: 13 216 hcpa nl

NORWAY

Hewlett-Packard Norge A/S
Nesboen 13
Box 149
N-1344 Haslum
Tel. (02) 53 83 60
Telex: 16621 hpnas n

SWEDEN

Hewlett-Packard Sverige AB
Enghetsvägen 1-3
Fack
S-161 20 Bromma 20
Tel. (08) 730 05 50
Cable: MEASUREMENTS
Stockholm
Telex: 10721

Hewlett-Packard Sverige AB
Ostra Vintergatan 22
S-702 40 Örebro
Tel. (019) 14 07 20
Hewlett-Packard Sverige AB
Frottalsgatan 30
S-421 32 Vasträ Frolunda
Tel. (031) 49 09 50
Telex: 10721 Via Bromma Office

SWITZERLAND

Hewlett-Packard (Schweiz) AG
Zürcherstrasse 20
P.O. Box 307
CH-8952 Schlieren-Zürich
Tel. (01) 730 52 40/730 18 21
Cable: HPAG CH
Telex: 53933 hpag ch

Hewlett-Packard (schweiz) AG
Château Bloc 19
CH-1219 Le Lignon-Geneva
Tel. (022) 96 03 22
Cable: HEWPAKAG Geneva
Telex: 27 333 hpag ch

SYRIA

Medical/Calculator only
Sawah & Co.
Place Azém
B.P. 2308
SYR-Damascus
Tel. 16367, 19697, 14268
Cable: SAWAH, Damascus
Telex: 30439

TURKEY

Telekom Engineering Bureau
P.O. Box 437
Beyoglu
P.O. Box 101000
Moscow
Tel. 49 40 40
Cable: TELEMATON Istanbul
Telex: 23609

UNITED KINGDOM

Hewlett-Packard Ltd.
King Street Lane
GB-Winnerh, Wokingham
Berk. RG11 5AR
Tel. (0734) 78 47 74
Cable: Hewlett-Packard London
Telex: 847178-9

Hewlett-Packard Ltd.
Trafalgar House
Hawthorn Road
Aldershot
Cheshire WA14 1NU
Tel. (061) 928 6422
Telex: 668068

Hewlett-Packard Ltd.
Lygon Court
Hewlett-Packard Ltd.
Lygon Court
Hewlett-Packard Ltd.
Lygon Court
Hewlett-Packard Ltd.
Lygon Court

Hewlett-Packard Ltd.
Lygon Court
Hewlett-Packard Ltd.
Lygon Court
Hewlett-Packard Ltd.
Lygon Court
Hewlett-Packard Ltd.
Lygon Court

Hewlett-Packard Ltd.
Lygon Court
Hewlett-Packard Ltd.
Lygon Court
Hewlett-Packard Ltd.
Lygon Court
Hewlett-Packard Ltd.
Lygon Court

Hewlett-Packard Ltd.
Lygon Court
Hewlett-Packard Ltd.
Lygon Court
Hewlett-Packard Ltd.
Lygon Court
Hewlett-Packard Ltd.
Lygon Court

Hewlett-Packard Ltd.
Lygon Court
Hewlett-Packard Ltd.
Lygon Court
Hewlett-Packard Ltd.
Lygon Court
Hewlett-Packard Ltd.
Lygon Court

Hewlett-Packard Ltd.
Lygon Court
Hewlett-Packard Ltd.
Lygon Court
Hewlett-Packard Ltd.
Lygon Court
Hewlett-Packard Ltd.
Lygon Court

Hewlett-Packard Ltd.
Lygon Court
Hewlett-Packard Ltd.
Lygon Court
Hewlett-Packard Ltd.
Lygon Court
Hewlett-Packard Ltd.
Lygon Court

Hewlett-Packard Ltd.
Lygon Court
Hewlett-Packard Ltd.
Lygon Court
Hewlett-Packard Ltd.
Lygon Court
Hewlett-Packard Ltd.
Lygon Court

Hewlett-Packard Ltd.
Lygon Court
Hewlett-Packard Ltd.
Lygon Court
Hewlett-Packard Ltd.
Lygon Court
Hewlett-Packard Ltd.
Lygon Court

Hewlett-Packard Ltd.
Lygon Court
Hewlett-Packard Ltd.
Lygon Court
Hewlett-Packard Ltd.
Lygon Court
Hewlett-Packard Ltd.
Lygon Court

Hewlett-Packard Ltd.
Wedg House
799, London Road
GB-Thornton Heath
Surrey CR4 6XJ
Tel. (01) 684 0103/8
Telex: 946825

Hewlett-Packard Ltd.
c/o Makro
South Service wholesale Centre
Wear Industrial Estate
Washington
GB-New Town, County Durham
Tel. Washington 464001 ext. 57/58

Hewlett-Packard Ltd.
10, Wesley St.
GB-Castleford
West Yorkshire WF10 1AE
Tel. (09775) 50402
Telex: 557355

Hewlett-Packard Ltd.
1, Wallace Way
GB-Hitchin
Herts
Tel. (0462) 52824/56704
Telex: 825981

Hewlett-Packard Ltd.
2C, Avonbeg Industrial Estate
Long Mile Road
DUBLIN 12
Tel. Dublin 509458
Telex: 30439

USSR
Hewlett-Packard
Representative Office USSR
Pokrovsky Boulevard 4-17-KW 12
Moscow 101000
Tel. 294-2024
Telex: 7582 hewpak su

YUGOSLAVIA
Iskra-standard/Hewlett-Packard
Miklosiceva 38/VII
61000 Ljubljana
Tel. 31 58 79/32 16 74
Telex: 31583

SOCIALIST COUNTRIES
NOT SHOWN PLEASE
CONTACT:
Hewlett-Packard Ges.m.b.H.
P.O. Box 7
A-1205 Vienna, Austria
Tel. (0222) 35 16 21 to 27
Cable: HEWPAK Vienna
Telex: 75923 hewpak a

MEDITERRANEAN AND
MIDDLE EAST COUNTRIES
NOT SHOWN PLEASE CONTACT:
Hewlett-Packard S.A.
Mediterranean and Middle
East Operations
35, Kolokotroni Street
Plata Kefallariou
GR-Kifissia-Athens, Greece
Tel. 8080337/359429
Telex: 21-6588
Cable: HEWPAKSA Athens

FOR OTHER AREAS
NOT LISTED CONTACT
Hewlett-Packard S.A.
7, rue du Bois-du-Lan
P.O. Box
CH-1217 Meyrin 2 - Geneva
Switzerland
Tel. (022) 82 70 00
Cable: HEWPAKSA Geneva
Telex: 2 24 86

UNITED STATES

ALABAMA

8290 Whitesburg Dr., S.E.
P.O. Box 4207
Huntsville 35802
Tel. (205) 881-4591
Medical Only
228 W. Valley Ave.,
Room 220
Birmingham 35209
Tel. (205) 942-2081/2

ARIZONA

2336 E. Magnolia St.
Phoenix 85034
Tel. (602) 244-1361
2424 East Aragon Rd.
Tucson 85706
Tel. (602) 294-3148

*ARKANSAS

Medical Service Only
P.O. Box 5646
Brady Station
Little Rock 72215
Tel. (501) 376-1844

CALIFORNIA

1430 East Orangefhorpe Ave.
Fullerton 92631
Tel. (714) 870-1000
3939 Lankershim Boulevard
North Hollywood 91604
Tel. (213) 877-1282
TWX: 910-499-2671

5400 West Rosecrans Blvd.
P.O. Box 92105
World Way Postal Center
Los Angeles 90009
Tel. (213) 970-7500

*LOS ANGELES

3003 Scott Boulevard
Santa Clara 95050
Tel. (408) 249-7000
TWX: 910-338-0518

*Ridgcrest
Tel. (714) 446-6165
646 W. North Market Blvd
Sacramento 95834
Tel. (916) 929-7222

9606 Aero Drive
P.O. Box 23333
San Diego 92123
Tel. (714) 279-3200

COLORADO
5800 South Ulster Parkway
Englewood 80110
Tel. (303) 771-3455

CONNECTICUT
12 Lunar Drive
New Haven 06525
Tel. (203) 389-6551
TWX: 710-465-2029

FLORIDA
P.O. Box 24210
2806 W. Oakland Park Blvd.
Ft. Lauderdale 33311
Tel. (305) 731-2020
*Jacksonville
Medical Service Only
Tel. (904) 398-0663
P.O. Box 13910
Ft. Lauderdale 33311
Tel. (714) 870-1000
Orlando 32809
Tel. (305) 859-2900
P.O. Box 12826
Pensacola 32575
Tel. (904) 476-8422

GEORGIA
P.O. Box 105005
Atlanta 30348
Tel. (404) 955-1500
TWX: 810-766-4890
Medical Service Only
*Augusta 30903
Tel. (404) 736-0592
P.O. Box 103
Warner Robins 31098
Tel. (912) 922-0449

MANUAL PART NO. 59310-90068
Printed in U.S.A. 4/78



Sales and service from 172 offices in 65 countries.
11000 Wolfe Road, Cupertino, California 95014